

Instruction Execution Times

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Introduction

This appendix contains several tables that provide the instruction execution times for DL105 Micro PLCs. Many of the execution times depend on the type of data used with the instruction. Registers may be classified into the following types:

- Data (word) Registers
- Bit Registers

V-Memory Data Registers

Some V-memory locations are considered data registers, such as timer or counter current values. Standard user V memory is classified as a V-memory data register. Note that you can load a bit pattern into these types of registers, even though their primary use is for data registers. The following locations are data registers:

Data Registers	DL105
Timer Current Values	V0 – V77
Counter Current Values	V1000 – V1077
User Data Words	V2000 – V2377 V4000 – V4177

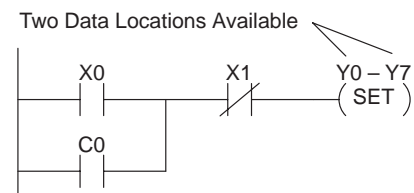
V-Memory Bit Registers

You may recall that some of the discrete points such as X, Y, C, etc. are automatically mapped into V memory. The following bit registers contain this data:

Bit Registers	DL105
Input Points (X)	V40400 – V 40407
Output Points (Y)	V40500 – V40507
Control Relays (C)	V40600 – V40617
Timer Status Bits	V41100 – V41103
Counter Status Bits	V41140 – V41143
Stages	V41000 – V41017

How to Read the Tables

Some instructions can have more than one parameter. For example, the SET instruction shown in the ladder program to the right can set a single point or a range of points.



In these cases, execution times that depend on the amount and type of parameters. The execution time tables list execution times for both situations, as shown below:

SET	1st #: X, Y, C, S	17.4 μ s
	2nd #: X, Y, C, S, (N pt)	12.0 μ s+5.4 μ sxN
RST	1st #: X, Y, C, S	19.5 μ s
	2nd #: X, Y, C, S, (N pt)	10.5 μ s+5.2 μ sxN

Execution depends on numbers of locations and types of data used

Instruction Execution Times

Boolean Instructions

Boolean Instructions		DL105	
Instruction	Legal Data Types	Execute	Not Execute
STR	X, Y, C, T, CT, S, SP	3.3 μ s	3.3 μ s
STRN	X, Y, C, T, CT, S, SP	3.9 μ s	3.9 μ s
OR	X, Y, C, T, CT, S, SP	2.7 μ s	2.7 μ s
ORN	X, Y, C, T, CT, S, SP	3.3 μ s	3.3 μ s
AND	X, Y, C, T, CT, S, SP	2.1 μ s	2.1 μ s
ANDN	X, Y, C, T, CT, S, SP	2.7 μ s	2.7 μ s
ANDSTR	None	1.2 μ s	1.2 μ s
ORSTR	None	1.2 μ s	1.2 μ s
OUT	X, Y, C	3.4 μ s	3.4 μ s
OROUT	X, Y, C	8.6 μ s	8.6 μ s
PD	X, Y, C	13.5 μ s	13.5 μ s
SET	1st #: X, Y, C, S 2nd #: X, Y, C, S (N pt)	17.4 μ s 12.0 μ s+5.4 μ sxN	6.8 μ s 6.8 μ s
RST	1st #: T, CT 2nd #: T, CT (N pt)	31.6 μ s 17 μ s+14.6 μ sxN	6.8 μ s 6.8 μ s
PAUSE	1wd: Y 2wd: Y (N points)	19.0 μ s 15 μ s+4 μ s x N	19.0 μ s 15 μ s+4 μ s x N
RST	1st #: X, Y, C, S 2nd #: X, Y, C, S (N pt)	17.7 μ s 10.5 μ s+5.2 μ sxN	6.8 μ s 6.8 μ s

Comparative Boolean Instructions

Comparative Boolean Instructions		DL105	
Instruction	Legal Data Types	Execute	Not Execute
STRE	1st	2nd	
	V: Data Reg.	V:Data Reg.	77 μ s
		V:Bit Reg.	158 μ s
		K:Constant	57 μ s
	V: Bit Reg.	V:Data Reg.	158 μ s
		V:Bit Reg.	240 μ s
STRNE		K:Constant	139 μ s
	1st	2nd	
	V: Data Reg.	V:Data Reg.	77 μ s
		V:Bit Reg.	158 μ s
		K:Constant	57 μ s
	V: Bit Reg.	V:Data Reg.	158 μ s
		V:Bit Reg.	240 μ s
		K:Constant	139 μ s

Comparative Boolean (cont.)			DL105	
Instruction	Legal Data Types		Execute	Not Execute
ORE	1st	2nd		
	V: Data Reg.	V:Data Reg.	75 μ s	12.0 μ s
		V:Bit Reg.	158 μ s	12.0 μ s
		K:Constant	55 μ s	12.0 μ s
	V: Bit Reg.	V:Data Reg.	158 μ s	12.0 μ s
		V:Bit Reg.	239 μ s	12.0 μ s
		K:Constant	137 μ s	12.0 μ s
ORNE	1st	2nd		
	V: Data Reg.	V:Data Reg.	75 μ s	12.0 μ s
		V:Bit Reg.	158 μ s	12.0 μ s
		K:Constant	55 μ s	12.0 μ s
	V: Bit Reg.	V:Data Reg.	158 μ s	12.0 μ s
		V:Bit Reg.	239 μ s	12.0 μ s
		K:Constant	137 μ s	12.0 μ s
ANDE	1st	2nd		
	V: Data Reg.	V:Data Reg.	75 μ s	12.0 μ s
		V:Bit Reg.	158 μ s	12.0 μ s
		K:Constant	55 μ s	12.0 μ s
	V: Bit Reg.	V:Data Reg.	158 μ s	12.0 μ s
		V:Bit Reg.	239 μ s	12.0 μ s
		K:Constant	137 μ s	12.0 μ s
ANDNE	1st	2nd		
	V: Data Reg.	V:Data Reg.	75 μ s	12.0 μ s
		V:Bit Reg.	158 μ s	12.0 μ s
		K:Constant	55 μ s	12.0 μ s
	V: Bit Reg.	V:Data Reg.	158 μ s	12.0 μ s
		V:Bit Reg.	239 μ s	12.0 μ s
		K:Constant	137 μ s	12.0 μ s
STR	1st	2nd		
	T, CT	V:Data Reg.	78 μ s	13.8 μ s
		V:Bit Reg.	158 μ s	13.8 μ s
		K:Constant	57 μ s	13.8 μ s
	1st	2nd		
	V: Data Reg.	V:Data Reg.	78 μ s	13.8 μ s
		V:Bit Reg.	159 μ s	13.8 μ s
		K:Constant	57 μ s	13.8 μ s
	V: Bit Reg.	V:Data Reg.	159 μ s	13.8 μ s
		V:Bit Reg.	241 μ s	13.8 μ s
		K:Constant	139 μ s	13.8 μ s
STRN	1st	2nd		
	T, CT	V:Data Reg.	78 μ s	13.8 μ s
		V:Bit Reg.	158 μ s	13.8 μ s
		K:Constant	57 μ s	13.8 μ s
	1st	2nd		
	V: Data Reg.	V:Data Reg.	78 μ s	13.8 μ s
		V:Bit Reg.	159 μ s	13.8 μ s
		K:Constant	57 μ s	13.8 μ s
	V: Bit Reg.	V:Data Reg.	159 μ s	13.8 μ s
		V:Bit Reg.	241 μ s	13.8 μ s
		K:Constant	139 μ s	13.8 μ s

Comparative Boolean (cont.)			DL105	
Instruction	Legal Data Types		Execute	Not Execute
OR	1st T, CT	2nd V:Data Reg.	75 μ s	12.0 μ s
		V:Bit Reg.	158 μ s	12.0 μ s
		K:Constant	55 μ s	12.0 μ s
	1st V: Data Reg.	2nd V:Data Reg.	75 μ s	12.0 μ s
		V:Bit Reg.	158 μ s	12.0 μ s
		K:Constant	55 μ s	12.0 μ s
ORN	1st T, CT	2nd V:Data Reg.	75 μ s	12.0 μ s
		V:Bit Reg.	158 μ s	12.0 μ s
		K:Constant	55 μ s	12.0 μ s
	1st V: Data Reg.	2nd V:Data Reg.	75 μ s	12.0 μ s
		V:Bit Reg.	158 μ s	12.0 μ s
		K:Constant	55 μ s	12.0 μ s
AND	1st T, CT	2nd V:Data Reg.	76 μ s	12.0 μ s
		V:Bit Reg.	158 μ s	12.0 μ s
		K:Constant	55 μ s	12.0 μ s
	1st V: Data Reg.	2nd V:Data Reg.	75 μ s	12.0 μ s
		V:Bit Reg.	158 μ s	12.0 μ s
		K:Constant	55 μ s	12.0 μ s
ANDN	1st T, CT	2nd V:Data Reg.	76 μ s	12.0 μ s
		V:Bit Reg.	158 μ s	12.0 μ s
		K:Constant	55 μ s	12.0 μ s
	1st V: Data Reg.	2nd V:Data Reg.	76 μ s	12.0 μ s
		V:Bit Reg.	158 μ s	12.0 μ s
		K:Constant	55 μ s	12.0 μ s
	1st V: Bit Reg.	2nd V:Data Reg.	158 μ s	12.0 μ s
		V:Bit Reg.	240 μ s	12.0 μ s
		K:Constant	137 μ s	12.0 μ s
		V:Data Reg.	158 μ s	12.0 μ s
		V:Bit Reg.	240 μ s	12.0 μ s
		K:Constant	137 μ s	12.0 μ s

Immediate Instructions

Immediate Instructions		DL105	
Instruction	Legal Data Types	Execute	Not Execute
STRI	X	27 μ s	9.8 μ s
STRNI	X	26 μ s	8.6 μ s
ORI	X	27 μ s	9.8 μ s
ORNI	X	26 μ s	8.6 μ s
ANDI	X	25 μ s	8.0 μ s
ANDNI	X	24 μ s	6.8 μ s
OROUTI	Y	45 μ s	45 μ s
SETI	1st #: Y	25.5 μ s	6.8 μ s
	2nd #: Y (N pt)	5.5 μ s+20 x N	6.8 μ s
RSTI	1st #: Y	25.5 μ s	6.8 μ s
	2nd #: Y (N pt)	5 μ s+20.5 x N	6.8 μ s

Timer, Counter, Shift Register, EDRUM Instructions

Timer, Counter, Shift Register, and Drum Instructions			DL105	
Instruction	Legal Data Types		Execute	Not Execute
TMR	1st	2nd		
	T	V:Data Reg.	75 μ s	31 μ s
		V:Bit Reg.	158 μ s	31 μ s
		K:Constant	66 μ s	31 μ s
TMRF	1st	2nd		
	T	V:Data Reg.	75 μ s	31 μ s
		V:Bit Reg.	158 μ s	31 μ s
		K:Constant	66 μ s	31 μ s
TMRA	1st	2nd		
	T	V:Data Reg.	94 μ s	56 μ s
		V:Bit Reg.	304 μ s	264 μ s
		K:Constant	95 μ s	45 μ s
TMRAF	1st	2nd		
	T	V:Data Reg.	98 μ s	54 μ s
		V:Bit Reg.	304 μ s	264 μ s
		K:Constant	95 μ s	49 μ s
CNT	1st	2nd		
	CT	V:Data Reg.	68 μ s	61 μ s
		V:Bit Reg.	148 μ s	141 μ s
		K:Constant	56 μ s	45 μ s
SGCNT	1st	2nd		
	CT	V:Data Reg.	57 μ s	64 μ s
		V:Bit Reg.	140 μ s	148 μ s
		K:Constant	46 μ s	53 μ s

Timer, Counter, Shift Register, and Drum Instructions Cont'd		DL105	
Instruction	Legal Data Types	Execute	Not Execute
UDC	1st 2nd CT V:Data Reg. V:Bit Reg. K:Constant	103 μ s 310 μ s 102 μ s	74 μ s 281 μ s 70 μ s
SR	C (N points to shift)	30 μ s+4.6 μ s xN	17.2 μ s
EDRUM	CT	320 μ s	221 μ s

Accumulator Data Instructions

Accumulator / Stack Load and Output Data Instructions		DL105	
Instruction	Legal Data Types	Execute	Not Execute
LD	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	68 μ s 149 μ s 62 μ s 169 μ s 256 μ s	8.4 μ s 8.4 μ s 8.4 μ s 8.4 μ s 8.4 μ s
LDD	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	72 μ s 266 μ s 64 μ s 172 μ s 373 μ s	8.4 μ s 8.4 μ s 8.4 μ s 8.4 μ s 8.4 μ s
LDF	1st 2nd X, Y, C, S K:Constant T, CT, SP (N pt)	77 μ s+6.2 μ s xN	10 μ s
LDA	O: (Octal constant for address)	58 μ s	8.4 μ s
OUT	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	60 μ s 132 μ s 162 μ s 239 μ s	8.4 μ s 8.4 μ s 8.4 μ s 8.4 μ s
OUTD	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	68 μ s 276 μ s 196 μ s 384 μ s	8.4 μ s 8.4 μ s 8.4 μ s 8.4 μ s
OUTF	1st 2nd X, Y, C K:Constant (N pt)	36 μ s+7.6 μ s xN	8 μ s
POP	None	55 μ s	7.2 μ s

Logical
Instructions

Logical (Accumulator) Instructions		DL105	
Instruction	Legal Data Types	Execute	Not Execute
AND	V:Data Reg. V:Bit Reg.	63 μ s 261 μ s	10.4 μ s 10.4 μ s
ANDD	K:Constant	53 μ s	8.4 μ s
OR	V:Data Reg. V:Bit Reg.	59 μ s 257 μ s	10.4 μ s 10.4 μ s
ORD	K:Constant	49 μ s	8.4 μ s
XOR	V:Data Reg. V:Bit Reg.	60 μ s 257 μ s	10.4 μ s 10.4 μ s
XORD	K:Constant	49 μ s	8.4 μ s
CMP	V:Data Reg. V:Bit Reg.	59 μ s 259 μ s	10.4 μ s 10.4 μ s
CMPD	V:Data Reg. V:Bit Reg. K:Constant	63 μ s 257 μ s 54 μ s	8.4 μ s 8.4 μ s 8.4 μ s

Math Instructions

Math Instructions (Accumulator)		DL105	
Instruction	Legal Data Types	Execute	Not Execute
ADD	V:Data Reg. V:Bit Reg.	198 μ s 397 μ s	10.6 μ s 10.6 μ s
ADDD	V:Data Reg. V:Bit Reg. K:Constant	198 μ s 397 μ s 188 μ s	8.4 μ s 8.4 μ s 8.4 μ s
SUB	V:Data Reg. V:Bit Reg.	200 μ s 397 μ s	10.6 μ s 10.6 μ s
SUBD	V:Data Reg. V:Bit Reg. K:Constant	198 μ s 392 μ s 190 μ s	8.4 μ s 8.4 μ s 8.4 μ s
MUL	V:Data Reg. V:Bit Reg. K:Constant	497 μ s 483 μ s 487 μ s	10.6 μ s 10.6 μ s 8.4 μ s
DIV	V:Data Reg. V:Bit Reg. K:Constant	909 μ s 1108 μ s 899 μ s	10.6 μ s 10.6 μ s 8.4 μ s
INCB	V:Data Reg. V:Bit Reg.	83 μ s 349 μ s	10.4 μ s 10.4 μ s
DECB	V:Data Reg. V:Bit Reg.	82 μ s 351 μ s	10.4 μ s 10.4 μ s

Bit Instructions

Bit Instructions (Accumulator)		DL105	
Instruction	Legal Data Types	Execute	Not Execute
SHFR	V:Data Reg. (N bits)	44 μ s+14.6 x N	10.4 μ s
	V:Bit Reg. (N bits)	243 μ s+14.6 x N	10.4 μ s
	K:Constant (N bits)	34 μ s+14.6 x N	8.4 μ s
SHFL	V:Data Reg. (N bits)	44 μ s+14.6 x N	10.4 μ s
	V:Bit Reg. (N bits)	243 μ s+14.6 x N	10.4 μ s
	K:Constant (N bits)	34 μ s+14.6 x N	8.4 μ s
ENCO	None	62 μ s	7.2 μ s
DECO	None	34 μ s	7.2 μ s

Number Conversion Instructions

Number Conversion Instructions (Accumulator)		DL105	
Instruction	Legal Data Types	Execute	Not Execute
BIN	None	359 μ s	7.2 μ s
BCD	None	403 μ s	7.2 μ s
INV	None	27 μ s	5.0 μ s

Table Instructions

Table Instructions		DL105	
Instruction	Legal Data Types	Execute	Not Execute
MOV	Move V:data reg. to V:data reg.	450 μ s+17 x N	6.2 μ s
	Move V:bit reg. to V:data reg.	430 μ s+244 x N	6.2 μ s
	Move V:data reg to V:bit reg.	460 μ s+215 x N	6.2 μ s
	Move V:bit reg. to V:bit reg.	490 μ s+448 x N	6.2 μ s
	N= #of words		
MOVMC	Move V:Data Reg. to E ²	—	—
	Move V:Bit Reg. to E ²	—	—
	Move from E ² to V:Data Reg.	250 μ s+201xN	6.2 μ s
	Move from E ² to V:Bit Reg.	—	—
	N= #of words		
LDLBL	K	58 μ s	8.4 μ s

CPU Control Instructions

CPU Control Instructions		DL105	
Instruction	Legal Data Types	Execute	Not Execute
NOP	None	0 μ s	0 μ s
END	None	27 μ s	27 μ s
STOP	None	16 μ s	5 μ s

Program Control Instructions

Program Control Instructions		DL105	
Instruction	Legal Data Types	Execute	Not Execute
MLS	K (1–7)	12 μ s	12 μ s
MLR	K (0–6) N= 1 to 7	13 μ s + 2.4 x N	13 μ s + 2.4 x N

Interrupt Instructions

Interrupt Instructions		DL105	
Instruction	Legal Data Types	Execute	Not Execute
ENI	None	9 μ s	5 μ s
DISI	None	8 μ s	5 μ s
INT	O0	0 μ s	0 μ s
IRT	None	1.6 μ s	—

Message Instructions

Message Instructions		DL105	
Instruction	Legal Data Types	Execute	Not Execute
FAULT	V:Data Reg. V:Bit Reg. K:Constant	171 μ s 253 μ s 2798 μ s	8.4 μ s 8.4 μ s 8.4 μ s
DLBL	K	0 μ s	0 μ s
NCON	K	0 μ s	0 μ s
ACON	K	0 μ s	0 μ s

RLL^{PLUS} Instructions

RLL ^{PLUS} Instructions		DL105	
Instruction	Legal Data Types	Execute	Not Execute
ISG	S	31 μ s	32 μ s
SG	S	31 μ s	32 μ s
JMP	S	14 μ s	8 μ s