MELSEC Q Series

User's Manual
Multiple CPU System

Q00CPU
Q01CPU
Q02CPU
Q02HCPU
Q06HCPU
Q12HCPU
Q25HCPU
Q12PHCPU
Q25PHCPU
Q12PRHCPU
Q25PRHCPU
Q02UCPU
Q03UDCPU
Q04UDHCPU
Q06UDHCPU

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010807
Versione E

MITSUBISHI ELECTRIC INDUSTRIAL AUTOMATION

QCPU

MITSUBISHI

User's Manual

(Multiple CPU System)

Mitsubishi
Programmable Controller

MELSEC-Q

Q00CPU	***Q12PHCPU***
Q01CPU	***Q25PHCPU***
Q02CPU	***Q02UCPU***
Q02HCPU	***Q03UDCPU***
Q06HCPU	***Q04UDHCPU***
Q12HCPU	***Q06UDHCPU***
Q25HCPU	

●SAFETY PRECAUTIONS●

(Always read these instructions before using this equipment.)

Before using this product, please read this manual and the relevant manuals introduced in this manual carefully and pay full attention to safety to handle the product correctly.
In this manual, the safety instructions are ranked as "DANGER" and "CAUTION".

DANGER	Indicates that incorrect handling may cause hazardous conditions, resulting in death or severe injury.
CAUTION	Indicates that incorrect handling may cause hazardous conditions, resulting in medium or slight personal injury or physical damage.

Note that the CAUTION level may lead to a serious consequence according to the circumstances. Always follow the instructions of both levels because they are important to personal safety.

Please save this manual to make it accessible when required and always forward it to the end user.

[Design Precautions]

DANGER

- Install a safety circuit external to the PLC that keeps the entire system safe even when there are problems with the external power supply or the PLC module. Otherwise, trouble could result from erroneous output or erroneous operation.
  (1) Outside the PLC, construct mechanical damage preventing interlock circuits such as emergency stop, protective circuits, positioning upper and lower limits switches and interlocking forward/ reverse operations.
  (2) When the PLC detects the following problems,
  it will stop calculation and turn off all output in the case of (a).
  In the case of (b), it will hold or turn off all output according to the parameter setting.
  Note that the AnS/A series module will turn off the output in either of cases (a) and (b).

	Q series module	AnS/A series module
(a) The power supply module has over currentprotection equipment and over voltage protection equipment.	Output OFF	Output OFF
(b) The CPU module self-diagnosis functions, such as the watchdog timer error, detect problems.	Hold or turn off all output according to the parameter setting.	Output OFF

  In addition, all output will be turned on when there are problems that the PLC CPU cannot detect, such as in the I/O controller. Build a fail safe circuit exterior to the PLC that will make sure the equipment operates safely at such times.
  Refer to " LOADING AND INSTALLATION" in QCPU User's Manual (Hardware Design, Maintenance and Inspection) for example fail safe circuits.
  (3) Output could be left on or off when there is trouble in the outputs module relay or transistor. So build an external monitoring circuit that will monitor any single outputs that could cause serious trouble.

[Design Precautions]

DANGER

- When overcurrent which exceeds the rating or caused by short-circuited load flows in the output module for a long time, it may cause smoke or fire. To prevent this, configure an external safety circuit, such as fuse.

- Build a circuit that turns on the external power supply when the PLC main module power is turned on.
  If the external power supply is turned on first, it could result in erroneous output or erroneous operation.

- When there are communication problems with the data link, refer to the corresponding data link manual for the operating status of each station.
  Not doing so could result in erroneous output or erroneous operation.

- When connecting a peripheral device to the CPU module or connecting a personal computer or the like to the intelligent function module / special function module to exercise control (data change) on the running PLC, configure up an interlock circuit in the sequence program to ensure that the whole system will always operate safely.
  Also before exercising other control (program change, operating status change (status control)) on the running PLC, read the manual carefully and fully confirm safety.
  Especially for the above control on the remote PLC from an external device, an immediate action may not be taken for PLC trouble due to a data communication fault.
  In addition to configuring up the interlock circuit in the sequence program, corrective and other actions to be taken as a system for the occurrence of a data communication fault should be predetermined between the external device and PLC CPU.

CAUTION

- Do not bunch the control wires or communication cables with the main circuit or power wires, or install them close to each other.
  They should be installed 100 mm (3.94 inch) or more from each other.
  Not doing so could result in noise that would cause erroneous operation.

- When controlling items like lamp load, heater or solenoid valve using an output module, large current (approximately ten times greater than that present in normal circumstances) may flow when the output is turned OFF to ON.
  Take measures such as replacing the module with one having sufficient rated current.

[Installation Precautions]

⚠CAUTION

- Use the PLC in an environment that meets the general specifications contained in QCPU User's Manual (Hardware Design, Maintenance and Inspection).
  Using this PLC in an environment outside the range of the general specifications could result in electric shock, fire, erroneous operation, and damage to or deterioration of the product.

- While pressing the installation lever located at the bottom of module, insert the module fixing tab into the fixing hole in the base unit until it stops. Then, securely mount the module with the fixing hole as a supporting point.
  Incorrect loading of the module can cause a malfunction, failure or drop.
  When using the PLC in the environment of much vibration, tighten the module with a screw.
  Tighten the screw in the specified torque range.
  Undertightening can cause a drop, short circuit or malfunction.
  Overtightening can cause a drop, short circuit or malfunction due to damage to the screw or module.

- When installing extension cables, be sure that the base unit and the extension module connectors are installed correctly.
  After installation, check them for looseness.
  Poor connections could cause an input or output failure.

- Securely load the memory card into the memory card loading connector.
  After installation, check for lifting.
  Poor connections could cause an operation fault.

- Completely turn off the externally supplied power used in the system before mounting or removing the module. Not doing so could result in damage to the product.Note that the module can be changed online (while power is on) in the system that uses the CPU module compatible with online module change or on the MELSECNET/H remote I/O station.
  Note that there are restrictions on the modules that can be changed online(while power is on), and each module has its predetermined changing procedure.
  For details, refer to QCPU User's Manual (Hardware Design, Maintenance and Inspection) and the online module change section in the manual of the module compatible with online module change.

- Do not directly touch the module's conductive parts or electronic components.
  Touching the conductive parts could cause an operation failure or give damage to the module.

- When using the Motion CPU module or motion module, be sure to check that the combination of modules is correct before power-on.
  The product may be damaged if the combination is incorrect.
  For details, refer to the user's manual for the Motion CPU module.

[Wiring Precautions]

DANGER
● Completely turn off the externally supplied power used in the system when installing or placing wiring. Not completely turning off all power could result in electric shock or damage to the product. ● When turning on the power supply or operating the module after installation or wiring work, be sure that the module's terminal covers are correctly attached. Not attaching the terminal cover could result in electric shock.

DANGER

- Be sure to ground the FG terminals and LG terminals to the protective ground conductor.
  Not doing so could result in electric shock or erroneous operation.

- When wiring in the PLC, be sure that it is done correctly by checking the product's rated voltage and the terminal layout.
  Connecting a power supply that is different from the rating or incorrectly wiring the product could result in fire or damage.

- External connections shall be crimped or pressure welded with the specified tools, or correctly soldered.
  Imperfect connections could result in short circuit, fires, or erroneous operation.

- Tighten the terminal screws with the specified torque.
  If the terminal screws are loose, it could result in short circuits, fire, or erroneous operation.
  Tightening the terminal screws too far may cause damages to the screws and/or the module, resulting in fallout, short circuits, or malfunction.

- Be sure there are no foreign substances such as sawdust or wiring debris inside the module.
  Such debris could cause fires, damage, or erroneous operation.

- The module has an ingress prevention label on its top to prevent foreign matter, such as wire offcuts, from entering the module during wiring.
  Do not peel this label during wiring.
  Before starting system operation, be sure to peel this label because of heat dissipation.

- Install our PLC in a control panel for use.
  Wire the main power supply to the power supply module installed in a control panel through a distribution terminal block.
  Furthermore, the wiring and replacement of a power supply module have to be performed by a maintenance worker who acquainted with shock protection.
  (For the wiring methods, refer to QCPU User's Manual (Hardware Design, Maintenance and Inspection))

[Startup and Maintenance Precautions]

DANGER

- Do not touch the terminals while power is on.
  Doing so could cause shock or erroneous operation.

- Correctly connect the battery.
  Also, do not charge, disassemble, heat, place in fire, short circuit, or solder the battery.
  Mishandling of battery can cause overheating or cracks which could result in injury and fires.

- Switch off all phases of the externally supplied power used in the system when cleaning the module or retightening the terminal or module mounting screws.
  Not doing so could result in electric shock.
  Undertightening of terminal screws can cause a short circuit or malfunction.
  Overtightening of screws can cause damages to the screws and/or the module, resulting in fallout, short circuits, or malfunction.

[Startup and Maintenance Precautions]

⚠CAUTION

- The online operations conducted for the CPU module being operated, connecting the peripheral device (especially, when changing data or operation status), shall be conducted after the manual has been carefully read and a sufficient check of safety has been conducted.
  Operation mistakes could cause damage or problems with of the module.

- Do not disassemble or modify the modules.
  Doing so could cause trouble, erroneous operation, injury, or fire.

- Use any radio communication device such as a cellular phone or a PHS phone more than 25cm (9.85 inch) away in all directions of the PLC.
  Not doing so can cause a malfunction.

- Completely turn off the externally supplied power used in the system before mounting or removing the module. Not doing so could result in damage to the product.
  Note that the module can be changed online (while power is on) in the system that uses the CPU module compatible with online module change or on the MELSECNET/H remote I/O station.
  Note that there are restrictions on the modules that can be changed online (while power is on) , and each module has its predetermined changing procedure.
  For details, refer to QCPU User's Manual (Hardware Design, Maintenance and Inspection) and the online module change section in the manual of the module compatible with online module change.

- Do not mount/remove the module onto/from base unit more than 50 times (IEC61131-2-compliant), after the first use of the product.Failure to do so may cause the module to malfunction due to poor contact of connector.

- Do not drop or give an impact to the battery mounted to the module.
  Doing so may damage the battery, causing the battery fluid to leak inside the battery.
  If the battery is dropped or given an impact, dispose of it without using.

- Before touching the module, always touch grounded metal, etc. to discharge static electricity from human body, etc.
  Not doing so can cause the module to fail or malfunction.

[Disposal Precautions]

⚠CAUTION
● When disposing of this product, treat it as industrial waste.

[Transportation Precautions]

⚠CAUTION
● When transporting lithium batteries, make sure to treat them based on the transport regulations. (Refer to Appendix 1 for details of the controlled models.)

REVISIONS

The manual number is given on the bottom left of the back cover.

Print Date	Manual Number	Revision
Jun., 2004	SH(NA)-080485ENG-A	First edition
May, 2005	SH(NA)-080485ENG-B	Partial correction GENERIC TERMS AND ABBREVIATIONS, Chapter 1, Section 1.1, 2.1, 2.3, 2.4, 3.1, 3.3.1, 3.3.2, 3.4.1, 3.4.2, 3.8, 3.9, 3.10, 4.1.1, 4.1.2, 4.1.3, 6.1, 6.1.1, 7.1, 8.1, 8.2.2, 8.2.3, 8.2.4, 8.3.1, 8.3.4, Appendix 1.1
Aug., 2005	SH(NA)-080485ENG-C	Partial correction GENERIC TERMS AND ABBREVIATIONS, Section 2.1
Apr., 2007	SH(NA)-080485ENG-D	Universal model QCPU model addition Revision involving Universal model QCPU serial No.09012 Model addition Q02UCPU, Q03UDCPU, Q04UDHCPU, Q06UDHCPU, Q61P, QA65B, QA68B Partial correction SAFETY PRECAUTION, ABOUT MANUALS, GENERIC TERMS AND ABBREVIATIONS, Section 1.1, 1.2, 1.3, 2.1.1, 2.1.2, 2.1.3, 2.2, 2.3, 2.4, 3.1.1, 3.1.2, 3.1.3, Chapter 4, Section 4.1, 4.1.1, 4.1.2, 4.1.3, 4.1.4, 4.1.5, 4.3.2, 5.1, 5.2, 6.1, 6.1.3, 6.1.4, 6.1.7, 6.1.8, 7.1, 8.1, 8.2.1, 8.2.2
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Japanese Manual Version SH-080475-E

INTRODUCTION

Thank you for choosing the Mitsubishi MELSEC-Q Series of General Purpose Programmable Controllers.
Before using the equipment, please read this manual carefully to develop full familiarity with the functions and performance of the Q series PLC you have purchased, so as to ensure correct use.

CONTENTS

SAFETY PRECAUTIONS •••••••••• A - 1
REVISIONS •••••••••• A - 10
INTRODUCTION •••••••••• A - 11
CONTENTS •••••••••• A - 11
ABOUT MANUALS •••••••••• A - 14
HOW TO SEE THIS MANUAL •••••••••• A - 16
HOW TO USE THIS MANUAL •••••••••• A - 18
GENERIC TERMS AND ABBREVIATIONS •••••••••• A - 19

CHAPTER1 OUTLINE 1 - 1 to 1 - 30

1.1 What is multiple CPU system? •••••••••• 1 - 10
1.2 Features of multiple CPU system •••••••••• 1 - 15
1.3 Difference from single CPU system •••••••••• 1 - 21

CHAPTER2 SYSTEM CONFIGURATION 2 - 1 to 2 - 52

2.1 System configuration •••••••••• 2 - 1
2.1.1 System configuration using Basic model QCPU (Q00CPU, Q01CPU) •••••••••• 2 - 1
2.1.2 System configuration using High Performance model QCPU or Process CPU as CPU No.1 •••••••••• 2 - 9
2.1.3 System configuration using Universal model QCPU as CPU No.1 •••••••••• 2 - 24
2.2 Configuration of peripheral devices •••••••••• 2 - 38
2.3 Configurable device and available software •••••••••• 2 - 42
2.4 Precautions for system configuration •••••••••• 2 - 49

CHAPTER3 CONCEPT FOR MULTIPLE CPU SYSTEM 3 - 1 to 3 - 34

3.1 Mounting position of CPU module •••••••••• 3 - 1
3.1.1 When CPU No.1 is Basic model QCPU •••••••••• 3 - 1
3.1.2 When CPU No.1 is High Performance model QCPU or Process CPU •••••••••• 3 - 4
3.1.3 When CPU No.1 is Universal model QCPU •••••••••• 3 - 7
3.2 CPU No. of CPU module •••••••••• 3 - 12
3.3 Concept of I/O number assignment •••••••••• 3 - 14
3.3.1 I/O number assignment of each module •••••••••• 3 - 14
3.3.2 I/O number of each CPU module •••••••••• 3 - 16

3.4 Access range of CPU module and other modules •••••• 3 - 17
3.4.1 Access range with controlled module •••••• 3 - 17
3.4.2 Access range with non-controlled module •••••• 3 - 17
3.5 Access target under GOT connection •••••• 3 - 24
3.6 Access with instruction using link direct device •••••• 3 - 24
3.7 Access range of GX Developer •••••• 3 - 25
3.8 Clock data used by CPU module and intelligent function module •••••• 3 - 28
3.8.1 Clock data used by CPU module •••••• 3 - 28
3.8.2 Clock data used by intelligent function module •••••• 3 - 28
3.9 Resetting the multiple CPU system •••••• 3 - 29
3.10 Operation for CPU module stop error •••••• 3 - 30
3.11 Host CPU number of multiple CPU system •••••• 3 - 33

CHAPTER4 COMMUNICATIONS BETWEEN CPU MODULES 4 - 1 to 4 - 57

4.1 Communications between CPU modules using CPU shared memory •••••• 4 - 3
4.1.1 CPU shared memory •••••• 4 - 3
4.1.2 Communication by auto refresh using CPU shared memory •••••• 4 - 8
4.1.3 Communication by auto refresh using multiple CPU high speed transmission area •••••• 4 - 23
4.1.4 Communication using CPU shared memory by program •••••• 4 - 38
4.1.5 Communications between CPU modules when the error occurs •••••• 4 - 48
4.2 Communications with instructions dedicated to Motion CPU •••••• 4 - 49
4.2.1 Control instruction from QCPU to Motion CPU •••••• 4 - 49
4.3 Communication between multiple CPUs with dedicated instructions •••••• 4 - 51
4.3.1 Write/read of device data from QCPU to Motion CPU •••••• 4 - 51
4.3.2 Start of interrupt program from QCPU to PC CPU module •••••• 4 - 53
4.4 Multiple CPU Synchronous Interrupt •••••• 4 - 54
4.5 Multiple CPU Synchronized Boot-up •••••• 4 - 56

CHAPTER5 PROCESSING TIME OF QCPU IN MULTIPLE CPU SYSTEM 5 - 1 to 5 -11

5.1 Concept of Scan Time •••••• 5 - 1
5.2 Factors for prolonged Scan Time •••••• 5 - 3
5.3 Reducing processing time •••••• 5 - 10

CHAPTER6 PARAMETER ADDED FOR MULTIPLE CPU SYSTEM 6 - 1 to 6 - 9

6.1 Parameter list •••••• 6 - 1
6.1.1 Number of CPUs setting •••••• 6 - 6
6.1.2 Operating mode setting •••••• 6 - 8
6.1.3 Online module change setting •••••• 6 - 8
6.1.4 I/O settings outside of the group •••••• 6 - 8
6.1.5 Refresh setting •••••• 6 - 8
6.1.6 Control CPU settings •••••• 6 - 9
6.1.7 Multiple CPU synchronized boot-up •••••• 6 - 9
6.1.8 Multiple CPU high speed transmission area setting •••••• 6 - 9

CHAPTER7 PRECAUTIONS FOR USE OF AnS/A SERIES MODULE 7 - 1 to 7 - 5

7.1 Precautions for use of AnS/A series compatible module ••••• 7 - 1

CHAPTER8 STARTING UP THE MULTIPLE CPU SYSTEM 8 - 1 to 8 - 39

8.1 Flow-chart for Starting Up the Multiple CPU System ••••• 8 - 1

8.2 Setting Up the Multiple CPU System Parameters ••••• 8 - 3

8.2.1 Parameter setting for the Basic model QCPU,High Paformance model QCPU,ProCess CPU ••••• 8 - 3

8.2.2 Parameter setting for the Universal model QCPU ••••• 8 - 15

8.2.3 Reusing preset multiple CPU parameters ••••• 8 - 23

8.3 Communication program example using auto refresh ••••• 8 - 28

8.3.1 Program example for the Basic model QCPU High Performance model QCPU and Process CPU ••••• 8 - 28

8.3.2 Program example for the Universal model QCPU ••••• 8 - 34

APPENDICES App- 1 to App - 2

Appendix 1 Transportation Precautions ••••• App- 1

Appendix 1.1 Controlled models ••••• App- 1

Appendix 1.2 Transport guidelines ••••• App- 1

INDEX Index- 1 to Index- 2

ABOUT MANUALS

The following manuals are also related to this product.
In necessary, order them by quoting the details in the tables below.

Related Manuals

(1) Common to CPU modules

The following table indicates the related manuals common to the Basic model QCPU, High Performance model QCPU, Process CPU and Universal model QCPU.

Manual Name	Manual Number (Model Code)
QCPU User's Manual (Hardware Design, Maintenance and Inspection) This manual provides the specifications of the CPU modules, power supply modules, base units, extension cables, memory cards and others. (Sold separately)	SH-080483ENG
QCPU User's Manual (Function Explanation, Program Fundamentals) This manual explains the functions, programming methods, devices necessary to create programs with the QCPU. (Sold separately)	SH-080484ENG
QCPU (Q Mode)/QnACPU Programming Manual (Common Instructions) This manual describes how to use the sequence instructions and application instructions. (Sold separately)	SH-080039
QCPU (Q Mode)/QnACPU Programming Manual (SFC) This manual explains the system configuration, performance specifications, functions, programming, debugging, error codes and others of MELSAP3. (Sold separately)	SH-080041 (13JF60)
QCPU (Q Mode) Programming Manual (MELSAP-L) This manual describes the programming methods, specifications functions, and so on that are necessary to create the MELSAP-L type SFC program. (Sold separately)	SH-080076 (13JF61)
QCPU (Q Mode) Programming Manual (Structured Text) This manual describes the structured text language programming methods. (Sold separately)	SH-080366E (13JF68)

(2) Basic model QCPU

The following table indicates the related manuals of the Basic model QCPU other than the manuals indicated in "(1) Common to CPU modules".

Manual Name	Manual Number (Model Code)
QCPU (Q Mode)/QnACPU Programming Manual (PID Control Instructions) This manual describes the dedicated instructions used to exercise PID control. (Sold separately)	SH-080040 (13JF59)
Q Corresponding MELSEC Communication Protocol Reference Manual This manual explains the communication methods and control procedures through the MC protocol for the external devices to read and write data from/to the CPU module using the serial communication module/ Ethernet module. (Sold separately)	SH-080008 (13JF89)

(3) High Performance model QCPU

The following table indicates the related manuals of the High Performance model QCPU other than the manuals indicated in "(1) Common to CPU modules".

Manual Name	Manual Number (Model Code)
QCPU (Q Mode)/QnACPU Programming Manual (PID Control Instructions) This manual describes the dedicated instructions used to exercise PID control. (Sold separately)	SH-080040 (13JF59)

(4) Process CPU

The following table indicates the related manuals of the Process CPU other than the manuals indicated in "(1) Common to CPU modules".

Manual Name	Manual Number (Model Code)
QnPHCPU/QnPRHCPU Programming Manual (Process Control Instructions) This manual describes the programming procedures, device names, and other items necessary to implement PID control using process control instructions. (Sold separately)	SH-080316E (13JF67)

(5) Universal model QCPU

The following table indicates the related manuals of the Universal model QCPU other than the manuals indicated in "(1) Common to CPU modules".

Manual Name	Manual Number (Model Code)
QCPU (Q Mode)/QnACPU Programming Manual (PID Control Instructions) This manual describes the dedicated instructions used to exercise PID control. (Sold separately)	SH-080040 (13JF59)

POINT

When using a Motion CPU, and/or PC CPU module in a multiple CPU system configuration, also refer to the manual for each of them.

HOW TO SEE THIS MANUAL

CPU modules requiring precautions

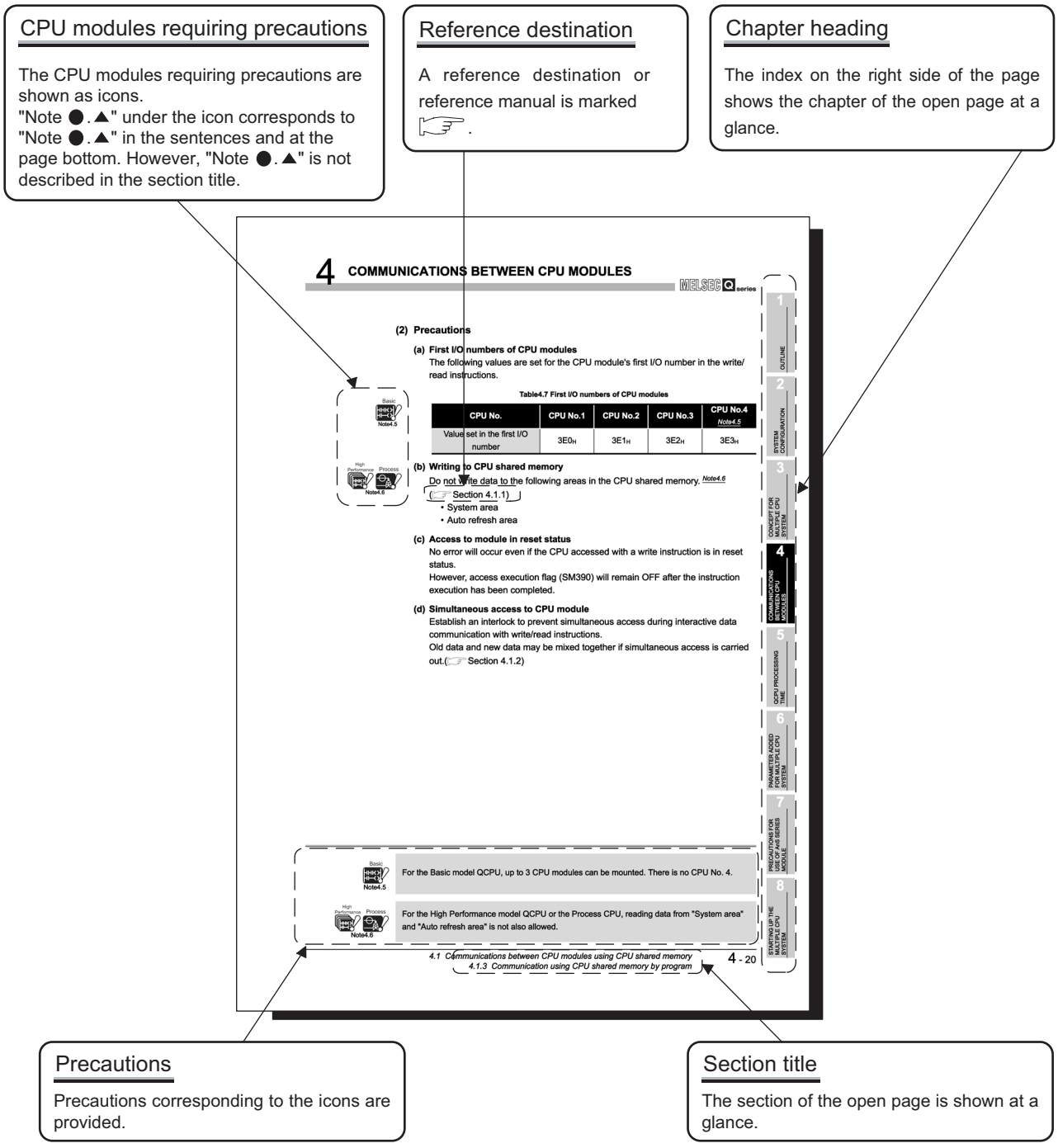
The CPU modules requiring precautions are shown as icons.
"Note ●.▲" under the icon corresponds to "Note ●.▲" in the sentences and at the page bottom. However, "Note ●.▲" is not described in the section title.

Reference destination

A reference destination or reference manual is marked ☞.

Chapter heading

The index on the right side of the page shows the chapter of the open page at a glance.



Precautions

Precautions corresponding to the icons are provided.

Section title

The section of the open page is shown at a glance.

Icon					Description
Basic model QCPU	High Performance model QCPU	Process CPU	Redundant CPU	Universal model QCPU	
Basic	High Performance	Process	Redundant	Universal	The ! marked icon indicates the CPU module does not support a part of the described functions.
Basic	High Performance	Process	Redundant	Universal	The × marked icon indicates the CPU module does not support all of the described functions.

In addition, this manual provides the following explanations.

POINT

Explains the matters to be especially noted, the functions and others related to the description on that page.

Remark

Provides the reference destination related to the description on that page and the convenient information.

HOW TO USE THIS MANUAL

This manual is designed for users to understand the multiple CPU system including information of the system configuration, functions, and communication with external devices that are required when the MELSEC-Q series PLC is used in the multiple CPU system.

This manual is composed of the following parts and explains:

1) Chapter 1 and 2	Overview and system configuration of the multiple CPU system
2) Chapter 3	Multiple CPU system concept
3) Chapter 4	Communications between CPU modules in the multiple CPU system
4) Chapter 5	Processing time in the multiple CPU system
5) Chapter 6	Parameters used in the multiple CPU system
6) Chapter 7	Precautions for use of the AnS series module in the multiple CPU system
7) Chapter 8	Startup of the multiple CPU system

Remark

(1) This manual does not include the specifications of the power supply module, base unit, extension cables, memory cards and batteries.
Refer to the following manual.
☞ QCPU User's Manual (Hardware Design, Maintenance and Inspection)

(2) For descriptions other than the multiple CPU system, refer to the following manual.
☞ QCPU User's Manual (Function Explanation, Program Fundamentals)

GENERIC TERMS AND ABBREVIATIONS

Unless otherwise specified, this manual uses the following generic terms and abbreviations to explain the Q series CPU modules.

Generic Term/Abbreviation	Description
Basic model QCPU	Generic term for Q00JCPU, Q00CPU, and Q01CPU modules.
High Performance model QCPU	Generic term for Q02CPU, Q02HCPU, Q06HCPU Q12HCPU, and Q25HCPU modules.
Process CPU	Generic term for Q12PHCPU, and Q25PHCPU.
Redundant CPU	Generic term for Q12PRHCPU, and Q25PRHCPU.
Universal model QCPU	Generic term for Q02UCPU, Q03UDCPU, Q04UDHCPU, and Q06UDHCPU.
QnHCPU	Generic term for Q02HCPU, Q06HCPU Q12HCPU, and Q25HCPU.
QnPHCPU	Generic term for Q12PHCPU, and Q25PHCPU.
Motion CPU	Generic term for Mitsubishi motion controllers, Q172CPUN, Q173CPUN, Q172HCPU, Q173HCPU, Q172DCPU, Q173DCPU.
PC CPU module	Generic term for MELSEC-Q series compatible PC CPU modules, PPC-CPU686(MS)-64, PPC-CPU686(MS)-128 and PPC-CPU852(MS)-512, manufactured by Contec Co., Ltd.
QCPU	Generic term for Basic model QCPU (except Q00JCPU), High Performance model QCPU, Process CPU, and Universal model QCPU.
CPU module	Generic term for QCPU, motion CPU, and PC CPU modules.
Q series	Abbreviation for Mitsubishi MELSEC-Q series Programmable Controller.
AnS series	Other name for compact types of Mitsubishi MELSEC-A series Programmable Controller.
A series	Other name for Large types of Mitsubishi MELSEC-A series Programmable Controller.
GX Developer	Product name for Q series compatible SW□D5C-GPPW-E type GPP function software package. □ indicates the version. For GX Developer versions available for the multiple CPU system, refer to “System Configuration” in this manual.
Q3□B	Generic term for Q33B, Q35B, Q38B and Q312B main base units on which QCPU, Q series power supply module, I/O modules and intelligent function module can be mounted.
Q3□SB	Generic term for Q32SB, Q33SB and Q35SB slim type main base units on which Basic model QCPU (except Q00JCPU), High Performance model QCPU, Universal model QCPU, slim type power supply module, I/O module, and intelligent function module can be mounted.
Q3□RB	Other name for Q38RB redundant power supply base unit on which QCPU, redundant power supply module, Q series I/O module and intelligent function module can be mounted.
Q3□DB	Other name for Q38DB and Q312DB Multiple CPU high speed main base units on which QCPU, Q series power supply module, Q series I/O module, and intelligent function module can be mounted.
Q5□B	Generic term for Q52B and Q55B extension base unit on which the Q Series I/O, and intelligent function module can be mounted.
Q6□B	Generic term for Q63B, Q65B, Q68B and Q612B extension base unit on which Q series power supply module, I/O module, and intelligent function module can be mounted.
Q6□RB	Other name for Q68RB redundant power supply base unit on which Q series I/O modules, intelligent function module, and redundant power supply module can be mounted.

Generic Term/Abbreviation	Description
QA1S6□B	Generic term for QA1S65B and QA1S68B extension base units with AnS Series power supply module, I/O module, and special function module can be mounted.
QA6□B	Generic term for QA65B and QA68B extension base units with A Series power supply module, I/O module, and special function module can be mounted.
A5□B	Generic term for A52B, A55B, and A58B extension base units on which A series I/O module and special function module can be mounted without power supply.
A6□B	Generic term for A62B, A65B, and A68B extension base units on which A series I/O module and special function module can be mounted.
QA6ADP	Abbreviation for QA6ADP QA conversion adapter module.
QA6ADP+A5□B/A6□B	Abbreviation for A large type extension base unit on which QA6ADP is mounted.
Q6□P	Generic term for the Q series compatible Q61P-A1, Q61P-A2, Q61P, Q62P, Q63P, and Q64P power supply modules.
Q6□SP	Other name for the Q61SP slim type power supply module.
Q6□RP	Generic term for Q63RP, and Q64RP redundant power supply module.
A1S6□P	Generic term for the AnS series compatible A1S61PN, A1S62PN, and A1S63P power supply modules.
Main base unit	Generic term for Q3□B, Q3□SB, Q3□RB, and Q3□DB.
Extension base unit	Generic term for Q5□B, Q6□B, Q6□RB, QA1S6□B, QA6□B, and QA6ADP+A5□B/A6□B.
Slim type main base unit	Other name for Q3□SB.
Redundant main base unit	Other name for Q3□RB.
Redundant extension base unit	Other name for Q6□RB.
Redundant base unit	Generic term for redundant main base unit and redundant extension base unit.
Multiple CPU high speed main base unit	Other name for Q3□DB.
Base unit	Generic term for main base unit, extension base unit, slim type main base unit, redundant main base unit, redundant extension base unit and multiple CPU high speed main base unit.
Extension cable	Generic term for QC05B, QC06B, QC12B, QC30B, QC50B, and QC100B extension cables.
Tracking cable	Generic term for QC10TR, and QC30TR tracking cables for Redundant CPU.
Q series power supply module	Generic term for Q61P-A1, Q61P-A2, Q61P, Q62P, Q63P, and Q64P power supply modules.
AnS series power supply module	Generic term for A1S61PN, A1S62PN, and A1S63P power supply modules.
A series power supply module	Generic term for A61P, A61PN, A62P, A63P, A61PEU, and A62PEU power supply modules.
Slim type power supply module	Other name for Q61SP slim type power supply module.
Redundant power supply module	Generic term for Q63RP, and Q64RP redundant power supply module.
Power supply module	Generic term for Q series power supply modules, AnS series power supply modules, A series power supply modules, slim type power supply module, and redundant power supply module.
Battery	Generic term for Q6BAT, Q7BAT and Q8BAT CPU module batteries, Q2MEM-BAT SRAM card battery, and Q3MEM-BAT SRAM card battery.
SRAM card	Generic term for Q2MEM-1MBS and Q2MEM-2MBS, Q3MEM-4MBS, and Q3MEM-8MBS type SRAM card.
Flash card	Generic term for Q2MEM-2MBF, and Q2MEM-4MBF type Flash card.
ATA card	Generic term for Q2MEM-8MBA, Q2MEM-16MBA, and Q2MEM-32MBA type ATA card.
Memory card	Generic term for SRAM card, Flash card and ATA card.

Generic Term/Abbreviation	Description
Motion module	Generic term for Q172LX, Q172EX, Q173PX, Q172DLX, Q172DEX, and Q172DPX modules dedicated to Mitsubishi motion controllers.
GOT	Generic term for Mitsubishi graphic operation terminal, GOT-A*** series and GOT-F*** series.
Single CPU system	System in which a QCPU (including Q00JCPU) is installed in CPU slot for control.
Multiple CPU system	System in which up to 4 CPUs can be installed to the main base unit for control.
CPU No.	Number assigned to the CPU modules in the multiple CPU system to distinguish each of them. CPU slot, slot 0, slot 1 and slot 2 are referred to as CPU No.1, No.2, No.3 and No.4 respectively.
CPU slot	Slot located next to and on the right of the power supply module in the main base unit.
Control CPU	CPU module that controls I/O modules, intelligent function modules mounted on the main base unit or extension base units. For example, when CPU No.2 controls a module installed in slot 3, CPU No.2 is the control CPU for the module in slot 3.
Non-control CPU	QCPUs other than control CPUs. For example, when CPU No.2 controls a module installed in slot 3, CPU No.1, 3 and 4 are non-control CPU for the module in slot 3.
Controlled module	I/O module or intelligent function module controlled by a control CPU. For example, when CPU No.2 controls a module installed in slot 3, the module in slot 3 is a controlled module for CPU No.2.
Non-controlled module (Non-group module)	I/O module or intelligent function module that is not a controlled module. For example, when CPU No.2 controls a module installed in slot 3, the module in slot 3 is a non-controlled module for CPU No.1, 3 and 4.
Dedicated instruction	Generic term for the motion CPU dedicated instruction and multiple CPU transmission dedicated instruction

CHAPTER1 OUTLINE

This manual describes the system configuration and the functions for use of the Q series CPU module (☞ (1) below) in the multiple CPU system.

Refer to the manual below for the power supply module, base unit, extension cable, memory card and battery.
☞ QCPU User's Manual (Hardware Design, Maintenance and Inspection)

Refer to the manual below for explanations other than the multiple CPU system.
☞ QCPU User's Manual (Function Explanation, Program Fundamentals)

(1) Applicable QCPU models

QCPUs described in this manual are as shown in Table1.1.

Table1.1 List of QCPUs described in this manual

QCPU type	QCPU model
Basic model QCPU	Q00CPU, Q01CPU
High Performance model QCPU	Q02CPU, Q02HCPU, Q06HCPU, Q12HCPU, Q25HCPU
Process CPU	Q12PHCPU, Q25PHCPU
Universal model QCPU	Q02UCPU, Q03UDCPU, Q04UDHCPU, Q06UDHCPU

(2) List of Q Series CPU Module manuals

The Q series CPU module manuals are as shown below.
For details such as manual numbers, refer to "About Manuals" in this manual.

(a) Basic model QCPU

Table1.2 List of user's manuals of Basic model QCPU

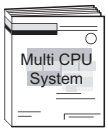
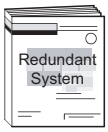
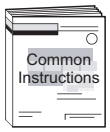
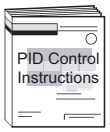
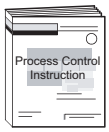
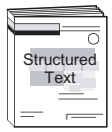
Purpose	QCPU (Q mode) CPU Module User's Manual (Hardware)	QCPU User's Manual (Hardware Design, Maintenance and inspection)	QCPU User's Manual (Function Explanation, Program Fundamentals)	QCPU User's Manual (Multiple CPU System)	QnPRHCPU User's Manual (Redundant System)
					
Confirmation of part names and specifications of the CPU module	Outline	Details	Outline		
Confirmation of connection methods for the power supply module, base unit and I/O module	Outline	Details			
Construction of the single CPU system (confirmation of start-up procedure and I/O number assignment)		Details			
Construction of the multiple CPU system (confirmation of start-up procedure and I/O number assignment)				Details	
Confirmation of the sequence program configuration and memory			Details		
Confirmation of the functions, parameters, and devices of the CPU module			Details		
Confirmation of the troubleshooting and error codes		Details			

Table1.3 List of programming manuals of Basic model QCPU

						
Purpose	**QCPU (Q mode)/ QnACPU Programming Manual (Common Instruction)**	**QCPU (Q mode)/ QnACPU Programming Manual (PID Control Instruction)**	**QnPHCPU/ QnPRHCPU Programming Manual (Process Control Instruction)**	**QCPU (Q mode)/ QnACPU Programming Manual (SFC)**	**QCPU (Q mode) Programming Manual (MELSAP-L)**	**QCPU (Q mode) Programming Manual (Structured Text)**
Confirmation of usage of sequence instructions, basic instructions, application instructions, etc.	Details					
Confirmation of dedicated instructions for PID control		Details				
Confirmation of MELSAP3's system configuration, performance specifications, functions, programming, debugging, and error codes				Details		
Confirmation of the programming method, specifications, functions, etc. required for SFC programming of the MELSAP-L type					Details	
Confirmation of the programming method of the structured text language						Details

(b) High Performance Model QCPU

Table1.4 List of user's manuals of High Performance model QCPU

Purpose	QCPU (Q mode) CPU Module User's Manual (Hardware)	QCPU User's Manual (Hardware Design, Maintenance and inspection)	QCPU User's Manual (Function Explanation, Program Fundamentals)	QCPU User's Manual (Multiple CPU System)	QnPRHCPU User's Manual (Redundant System)
	 (Packed)				
Confirmation of part names and specifications of the CPU module	Outline	Details	Outline		
Confirmation of connection methods for power supply module, base unit and I/O module	Outline	Details			
Construction of the single CPU system (confirmation of start-up procedure and I/O number assignment)		Details			
Construction of the multiple CPU system (confirmation of start-up procedure and I/O number assignment)				Details	
Confirmation of the sequence program configuration and memory			Details		
Confirmation of the functions, parameters, and devices of CPU module			Details		
Confirmation of the troubleshooting and error codes		Details			

Table1.5 List of programming manuals of High Performance model QCPU

Purpose	Common Instructions QCPU (Q mode)/ QnACPU Programming Manual (Common Instruction)	PID Control Instructions QCPU (Q mode)/ QnACPU Programming Manual (PID Control Instruction)	Process Control Instruction QnPHCPU/ QnPRHCPU Programming Manual (Process Control Instruction)	SFC QCPU (Q mode)/ QnACPU Programming Manual (SFC)	MELSAP-L QCPU (Q mode) Programming Manual (MELSAP-L)	Structured Text QCPU (Q mode) Programming Manual (Structured Text)
Confirmation of usage of sequence instructions, basic instructions, application instructions, etc.	Details					
Confirmation of dedicated instructions for PID control		Details				
Confirmation of MELSAP3's system configuration, performance specifications, functions, programming, debugging, and error codes				Details		
Confirmation of the programming method, specifications, functions, etc. required for SFC programming of the MELSAP-L type					Details	
Confirmation of the programming method of the structured text language						Details

(c) Process CPU

Table1.6 List of user's manuals of Process CPU

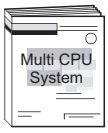
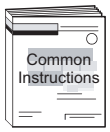
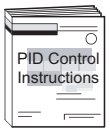
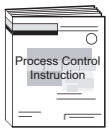
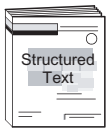
Purpose	QCPU (Q mode) CPU Module User's Manual (Hardware)	QCPU User's Manual (Hardware Design, Maintenance and inspection)	QCPU User's Manual (Function Explanation, Program Fundamentals)	QCPU User's Manual (Multiple CPU System)	QnPRHCPU User's Manual (Redundant System)
	 (Packed)				
Confirmation of part names and specifications of the CPU module	Outline	Details	Outline		
Confirmation of connection methods for power supply module, base unit and I/O module	Outline	Details			
Construction of the single CPU system (confirmation of start-up procedure and I/O number assignment)		Details			
Construction of the multiple CPU system (confirmation of start-up procedure and I/O number assignment)				Details	
Confirmation of sequence program configuration and memory			Details		
Confirmation of the functions, parameters, and devices of the CPU module			Details		
Confirmation of the troubleshooting and error codes		Details			

Table1.7 List of programming manuals of Process CPU

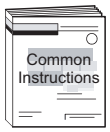
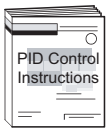
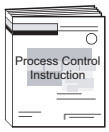
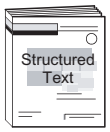
						
Purpose	**QCPU (Q mode)/ QnACPU Programming Manual (Common Instruction)**	**QCPU (Q mode)/ QnACPU Programming Manual (PID Control Instruction)**	**QnPHCPU/ QnPRHCPU Programming Manual (Process Control Instruction)**	**QCPU (Q mode)/ QnACPU Programming Manual (SFC)**	**QCPU (Q mode) Programming Manual (MELSAP-L)**	**QCPU (Q mode) Programming Manual (Structured Text)**
Confirmation of usage of sequence instructions, basic instructions, application instructions, etc.	Details					
Confirmation of dedicated instructions for process control			Details			
Confirmation of MELSAP3's system configuration, performance specifications, functions, programming, debugging and error codes				Details		
Confirmation of the programming method, specifications, functions etc. required for SFC programming of the MELSAP-L type					Details	
Confirmation of the programming method of the structured text language						Details

(d) Universal Model QCPU

Table1.8 List of user's manuals of Universal model QCPU

Purpose	QCPU (Q mode) CPU Module User's Manual (Hardware)	QCPU User's Manual (Hardware Design, Maintenance and inspection)	QCPU User's Manual (Function Explanation, Program Fundamentals)	QCPU User's Manual (Multiple CPU System)	QnPRHCPU User's Manual (Redundant System)
					
Confirmation of part names and specifications of the CPU module	Outline	Details	Outline		
Confirmation of connection methods for power supply module, base unit and I/O module	Outline	Details			
Construction of the single CPU system (confirmation of start-up procedure and I/O number assignment)		Details			
Construction of the multiple CPU system (confirmation of start-up procedure and I/O number assignment)				Details	
Confirmation of the sequence program configuration and memory			Details		
Confirmation of the functions, parameters, and devices of CPU module			Details		
Confirmation of the troubleshooting and error codes		Details			

Table1.9 List of programming manuals of Universal model QCPU

						
Purpose	**QCPU (Q mode)/ QnACPU Programming Manual (Common Instruction)**	**QCPU (Q mode)/ QnACPU Programming Manual (PID Control Instruction)**	**QnPHCPU/ QnPRHCPU Programming Manual (Process Control Instruction)**	**QCPU (Q mode)/ QnACPU Programming Manual (SFC)**	**QCPU (Q mode) Programming Manual (MELSAP-L)**	**QCPU (Q mode) Programming Manual (Structured Text)**
Confirmation of usage of sequence instructions, basic instructions, application instructions, etc.	Details					
Confirmation of dedicated instructions for PID control		Details				
Confirmation of MELSAP3's system configuration, performance specifications, functions, programming, debugging, and error codes				Details		
Confirmation of the programming method, specifications, functions, etc. required for SFC programming of the MELSAP-L type					Details	
Confirmation of the programming method of the structured text language						Details

1.1 What is multiple CPU system?

(1) Configuration of multiple CPU system

A multiple CPU system is a system in which more than one CPU module are mounted on several a main base unit in order to control the I/O modules and intelligent function modules.*1

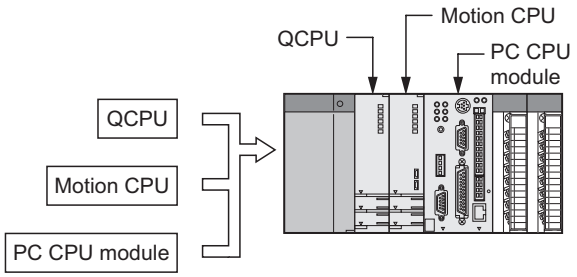


Diagram 1.1 Configuration of multiple CPU

* 1: A multiple CPU system can be configured with up to 3 CPU modules for a Basic model QCPU, Universal model QCPU (Q02UCPU) and up to 4 CPU modules for a High Performance model QCPU, Process CPU or Universal model QCPU (except Q02UCPU).

Applicable CPU modules are shown in Table1.10. Note1.1

Refer to Section 2.3 for the compatible version of each module.

Redundant Note1.1

Basic Note1.2

Table1.10 Applicable CPU modules

CPU module		Model
Q C P U	Basic model QCPU Note1.2	Q00CPU, Q01CPU
	High Performance model QCPU	Q02CPU,Q02HCPU,Q06HCPU,Q12HCPU, Q25HCPU
	Process CPU	Q12PHCPU,Q25PHCPU
	Universal model QCPU	Q02UCPU, Q03UDCPU,Q04UDHCPU,Q06UDHCPU
Motion CPU		Q172CPUN,Q173CPUN,Q172HCPU,Q173HCPU
		Q172DCPU,Q173DCPU
PC CPU module		CONTEC Co., Ltd.*2

Choose the CPU modules suitable for the system size and application to configure the system.

Some combinations of CPU modules in table 1.10 cannot be used.

Refer to Section 3.1 for combinations of configurable CPU modules.

* 2: For further information on PC CPU module, consult CONTEC Co.,Ltd.
Tel:+81-6-6472-7130

Remark

For details of the Motion CPU, and PC CPU module, refer to the manual of each CPU module.

Redundant Note1.1

The redundant CPU is not available for the multiple CPU system.

Basic Note1.2

The Q00JCPU is not available for the multiple CPU system.

(2) Method for controlling I/O module and intelligent function module

It is necessary to set (control CPU setup) which CPU modules are to control which I/O modules and intelligent function modules with a multiple CPU system.

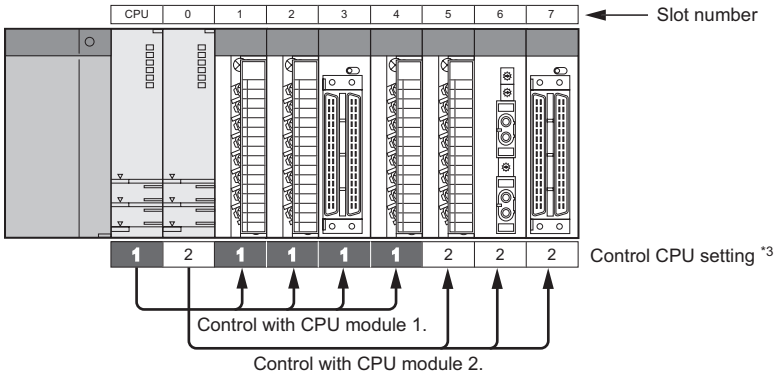


Diagram 1.2 Setting of control CPU

* 3: Indicates the grouping configuration on the GX Developer.
"1" on the CPU module indicates "CPU No.1," and "1" on the I/O module and intelligent function module indicates that their "Control CPU is the CPU No.1."

The CPU module that controls the I/O modules and intelligent function modules is called as a "Control CPU".
The I/O modules and intelligent function modules controlled by the control CPU are called "controlled modules".
Other modules not controlled by the control CPU are called as "non-controlled modules".

(3) Multiple CPU system setting

For control in the multiple CPU system, it is necessary to set up the "Number of mounted CPU modules" and the "Control CPU" with PLC parameters for all CPU modules mounted on the main base unit.

☞ QCPU User's Manual (Function Explanation, Program Fundamentals)

(4) Access range of multiple CPU system

In the multiple CPU system, the access ranges are different between the controlled module and the non-controlled module.

(a) Controlled module

The multiple CPU system's control CPU can refresh the I/O data of controlled modules and read/write the buffer memory data of intelligent function modules in the same way as in a single CPU system.

(b) Non-controlled module

It is possible to access non-controlled modules in the following ways.

- Refreshing the input for I/O modules, I/O composite module and intelligent function modules
  (the PLC parameter's multiple CPU setup is necessary.)
- Reading the intelligent function module's buffer memory.
- Downloading the output data from the output module, the I/O composite module and the intelligent function modules.
  (the PLC parameter's multiple CPU setup is necessary.)

However, it is not possible to access non-controlled modules in the following ways.

- Outputting data to output modules, I/O composite module and intelligent function modules.
- Writing data into the intelligent function module's buffer memory.

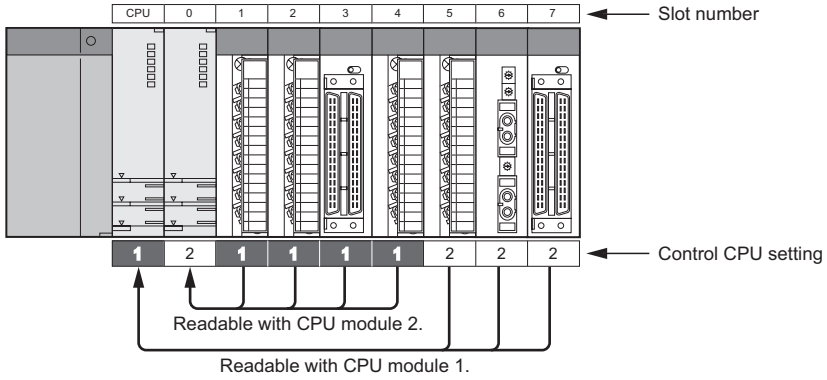


Diagram 1.3 Access to non-controlled module

(c) Range of access to other station's CPU module

To access to a CPU module on other station from GX Developer, access can be made through a network module controlled by any CPU module in the multiple CPU system.

When other station has multiple CPUs, specifying the CPU No. allows access to the desired CPU.

☞ User's manual for each network module

1.2 Features of multiple CPU system

(1) Multi-control system

(a) Configuration optimum for system

Since each system uses not only one QCPU but any combinations of the QCPU, Motion CPU, and PC CPU module according to the system, the development efficiency and ease of maintenance of the system can be enhanced.

(b) Module control

Each CPU module in the multiple CPU system controls the I/O module and intelligent function module on the base unit by each slot.

GX Developer groups the I/O modules and intelligent function modules controlled by each CPU module in the multiple CPU system.

(2) Sequence control and motion control systems can be configured on the same base.

In a Multiple CPU System consisting of the QCPU and Motion CPU, sequence control and motion control can be implemented together to achieve a high-level motion system.

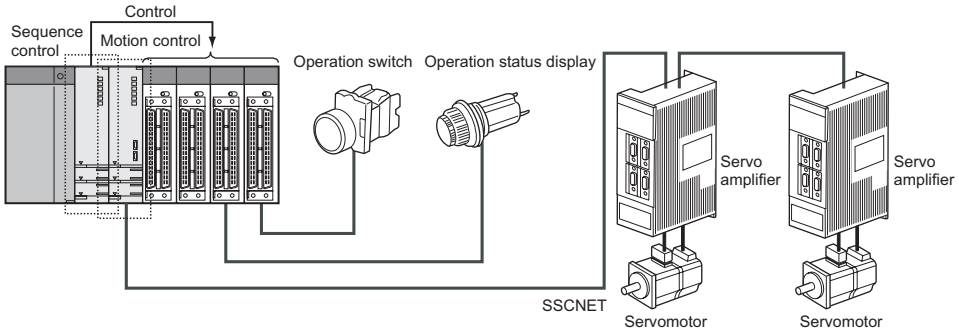


Diagram 1.4 Motion system configuration

Interaction with a motion controller for motion control is enhanced in the Universal model QCPU.

(a) Speeding up data transfer between multiple CPUs

Maximum 14 k word-data and a sequence program can be transferred between multiple CPUs with parallel processing. It enables high-speed data transfer independent of scan time, which leads to takt time shortening of equipment.

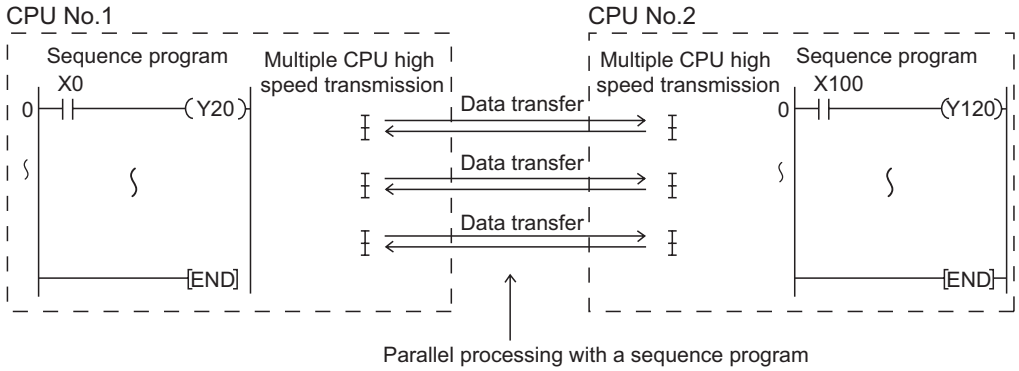


Diagram 1.5 Multiple CPU data transfer

POINT

Speeding up data transfer between multiple CPUs is available when the following CPU modules are used.

- Universal model QCPU (except Q02UCPU)
- Motion CPU (Q172DCPU, Q173DCPU)

(b) Enabling synchronous processing with a motion control

An interrupt program which is synchronized with the operation cycle of a motion controller (multiple CPU synchronous interrupt program) can be executed. Command I/O from a motion controller can be synchronized with the operation cycle of the motion controller, which enables high-speed data transfer independent of scan time.

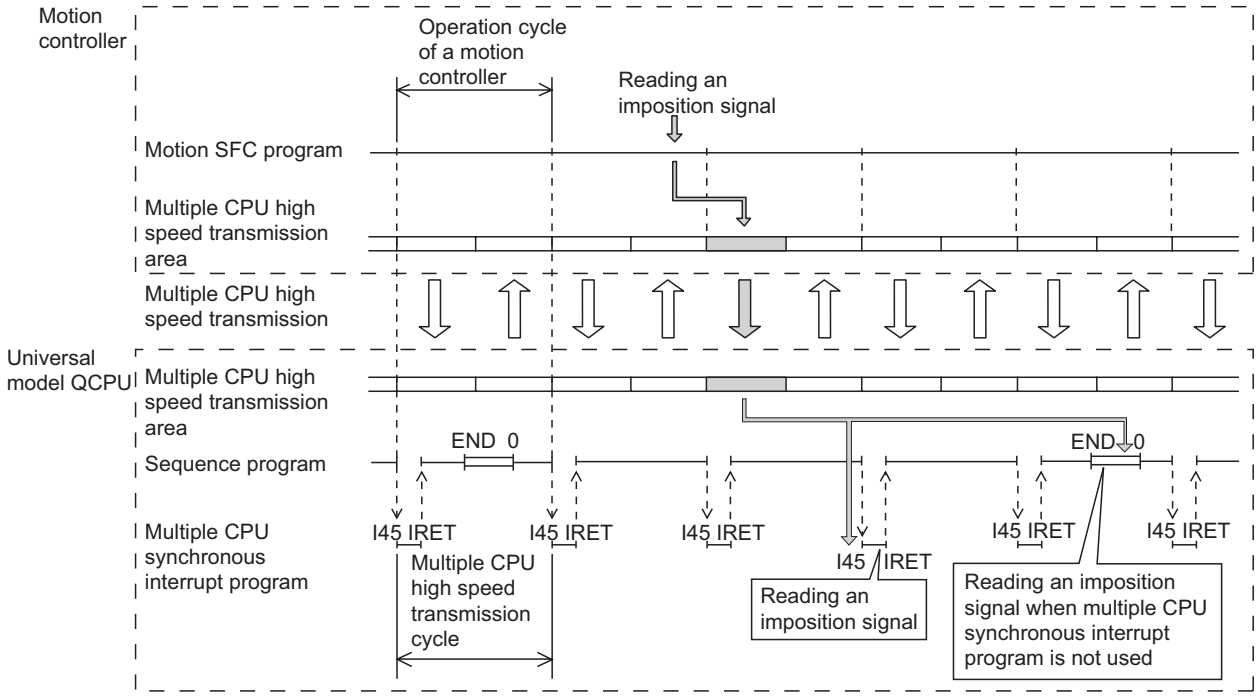


Diagram 1.6 Reading data using multiple CPU synchronous interrupt program

POINT

The synchronous processing with the Motion CPU is available when the following CPU modules are used.

- Universal model QCPU (except Q02UCPU)
- Motion CPU (Q172DCPU, Q173DCPU)

(c) Timing of data send/receive between the CPU modules can be checked

The sampling trace function of the Universal model QCPU enables to check the data send/receive timing with the Motion controller.
(Timing of data send/receive can be checked between the Universal model QCPUs.)
Using the sampling trace function facilitates to check the data send/receive timing between CPU modules, and reduces the debug time of the multiple CPU system.

Sampling trace result display by GX Developer

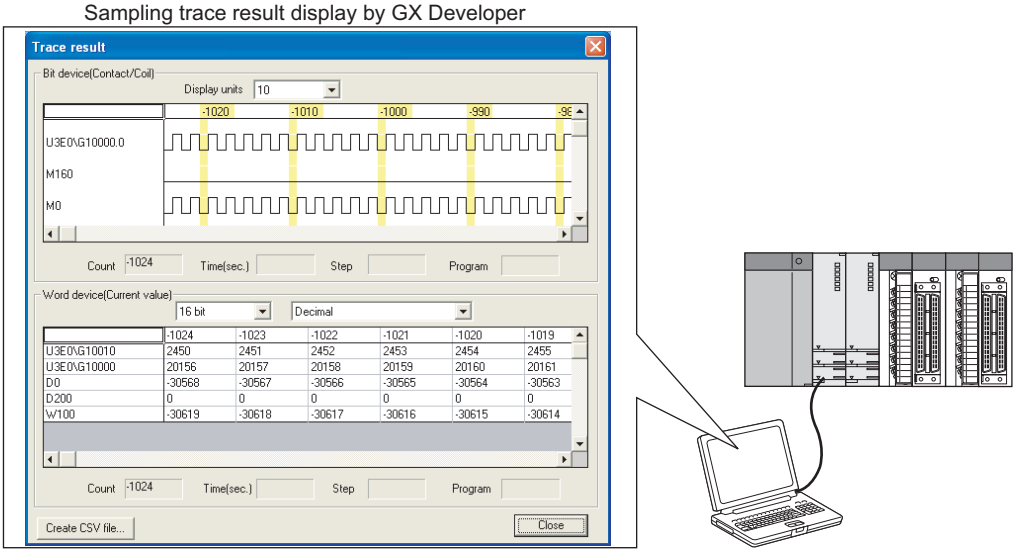


Diagram 1.7 Sampling trace at the time of configuring multiple CPU system

POINT

The sampling trace of the other CPU module data can be executed, specifying the following CPU modules.

- Universal model QCPU (except Q02UCPU)
- Motion CPU (Q172DCPU, Q173DCPU)

(3) System configuration based on load distribution.

(a) Distribution of processing

By distributing the high-load processing performed on a single QCPU over several CPU modules, it is possible to reduce the overall system scan time.

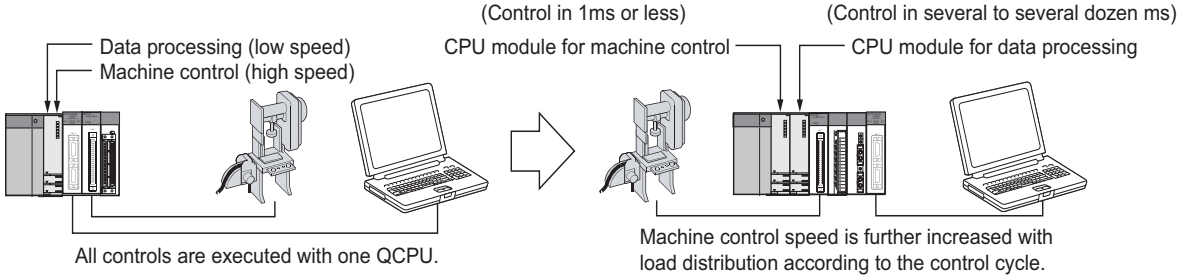


Diagram 1.8 Distribution of processing

(b) Distribution of memory

It is possible to increase the amount of memory used throughout the entire system by distributing the memory used over several CPU modules.

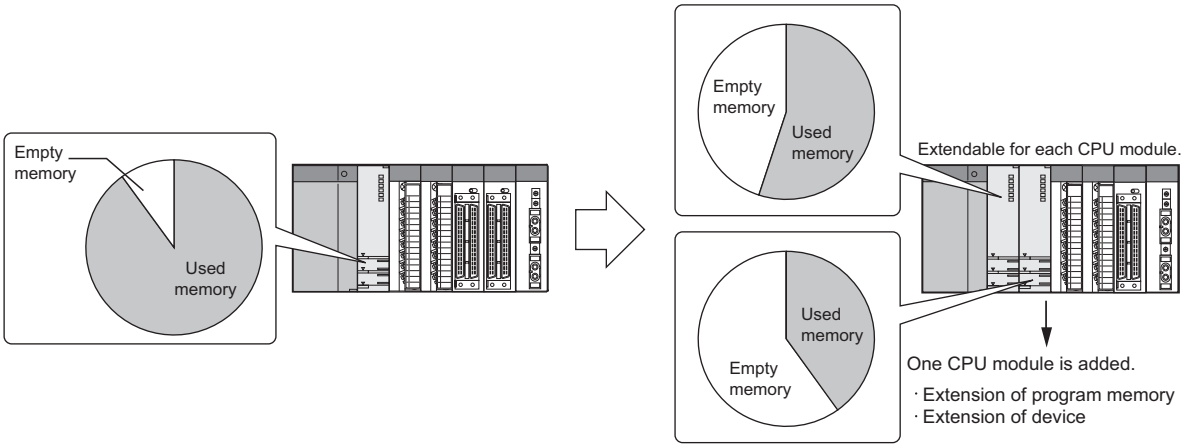


Diagram 1.9 Distribution of memory

(4) Enables system configuration through function distributing

By distributing the functions, control for production line A and control for production line B is performed on different CPU modules, allowing easy program development.

(5) Communication between CPU modules in the multiple CPU system

The following data transfer can be made between CPU modules in the multiple CPU system.

(a) Data transfer between CPU modules

The following data transfer can be made between CPU modules in the multiple CPU system.

(b) Reading other CPU data

The QCPU can use the FROM instruction/multiple CPU area device (U3En\G□) to read data from other CPU as necessary.

(c) Control instruction to Motion CPU

Instructions dedicated to the Motion CPU[*1] can be used to issue control commands from the QCPU to the Motion CPU.

(d) Read/write of Motion CPU's device data

The QCPU can issue instructions dedicated to communication between multiple CPUs[*2], to read or write device data from/to the Motion CPU.

(e) Event issue to PC CPU module

With the instruction dedicated to the communication between multiple CPUs[*2], an event can be issued from a QCPU to a PC CPU module.

* 1: Refer to the manual of the Motion CPU for instructions dedicated to Motion.
* 2: Refer to the manuals of Motion CPU and PC CPU module for instructions dedicated to the communication between multiple CPUs.

POINT

The Universal model QCPU(except Q02UCPU) allows executing the motion CPU dedicated instruction several times in the same scan.
Since the motion CPU dedicated instruction can be executed consecutively to different axis numbers, delay time of servo startup interval can be shortened.

1.3 Difference from single CPU system

Differences between the single CPU system and the multiple CPU system are described in this section.
Refer to the manuals below for the single CPU system.
☞ QCPU User's Manual (Hardware Design, Maintenance and Inspection)
☞ QCPU User's Manual (Function Explanation, Program Fundamentals)

(1) When using the Basic model QCPU

Table1.11 Difference from single CPU system

Item		Single CPU system	Multiple CPU system	Reference
System configuration	Maximum number of extension stages	4 stages		Section 2.1.1
	Maximum number of mountble I/O modules	25 - (No. of CPUs)*1, *2		
	Main base unit model	Q3□B, Q3□SB, Q3□RB, Q3□DB	Q3□B, Q3□SB, Q3□DB	
	Extension base unit model	Q5□B, Q6□B, Q6□RB	Q5□B, Q6□B	
	Extension cable type	QC05B, QC06B, QC12B, QC30B, QC50B, QC100B		
	Overall distance of extension cable	Within 13.2 m		
	Power supply module model	Q6□P, Q6□SP, Q6□RP	Q6□P, Q6□SP	
Available module	Basic model QCPU	Function version A or later	Function version B or later	Section 2.3
	I/O module	Function version A or later		
	Intelligent function module	Function version A or later	Function version B or later (Function version A or later for QD62, QD62D and QD62E. No version restriction for QI60.)	
Available software package	GX Developer	Version 7 or later	Version 8 or later	
	GX Configurator-AD	Version 1.10L or later*3		
	GX Configurator-DA	Version 1.10L or later*3		
	GX Configurator-SC	Version 1.10L or later		
	GX Configurator-CT	Version 1.10L or later*3		
	GX Configurator-TI	Version 1.10L or later*3		
	GX Configurator-TC	Version 1.10L or later		
	GX Configurator-FL	Version 1.10L or later		
	GX Configurator-QP	Version 2.10L or later		
	GX Configurator-PT	Version 1.10L or later		
	GX Configurator-AS	Version 1.13P or later		
	GX Configurator-MB	Version 1.00A or later		
	GX Configurator-DN	Version 1.10L or later		
Concept	CPU module mounting position and CPU No.	CPU slot only (no CPU No.)	CPU slot = CPU No. 1 Slot 0 = CPU No. 2 Slot 1 = CPU No. 3	Section 3.1.1
	I/O number assignment	Slot 0 is 00H.	The number assigned to the right of the CPU module placed in the rightmost position in the multiple CPU setting is 00H.*4	Section 3.1.1
	Restrictions on number of mountable modules	The number of mountable modules per CPU module is restricted depending on the module type.	The number of mountable modules per QCPU and per system is restricted depending on the module type.	Section 2.4

* 1: "No. of CPUs" indicates the number of CPU modules set in the "No. of PLCs" of the GX Developer.
It is 1 for the single CPU system.
* 2: When the PC CPU module is mounted on the multiple CPU system, the maximum number of mountble I/O modules is 25 - (No. of CPUs +1).
* 3: For some intelligent function modules, different version may be used.
* 4: When the PC CPU module is mounted, the slot to the right of the PC CPU module is 10H.

Table1.11 Difference from single CPU system (continued)

Item		Single CPU system	Multiple CPU system	Reference
Access range	Access from CPU module to other modules	All modules can be controlled.	Setting the relations between the CPU module and other modules with the PLC parameters (control CPU) is required.	Section 3.4
	Access from GOT	Accessible		Manuals for GOT
	Access with instruction using link direct	Accessible	Only control CPU is accessible.	Section 3.6
	Access to CC-Link	Accessible	Only control CPU is accessible.	CC-Link system master/local module manuals
	Access from peripheral devices	Accessible through RS-232 cable or via network.	Accessible through RS-232 cable or via network. For access when the Motion CPU, or PC CPU module is connected, refer to the relevant manual.	Section 2.2
Clock function	Clock data used by intelligent function module (QD75, etc.)	Clock data of the Basic model QCPU is used.	Clock data of the Basic model QCPU (CPU No. 1) is used.	Section 3.8
Operation	CPU module resetting operation	The entire system is reset by resetting the Basic model QCPU.	The entire system is reset by resetting the Basic model QCPU (CPU No. 1). (Resetting CPU No. 2 and 3 individually is not allowed.)	Section 3.9
	Operation for CPU module stop error	The system stops.	For a stop error of the Basic model QCPU of CPU No. 1, the multiple CPU system stops. (CPU modules No. 2 and 3 are in "MULTI CPU DOWN (Error code: 7000)" status. For a stop error occurred in CPU No. 2 or 3, the operation depends on the parameter setting of "Operation mode".	Section 3.10
Communication between CPU modules	Communication using CPU shared memory by auto refresh	----	Basic model QCPU = 320 points Motion CPU = 2048 points PC CPU module = 2048 points Total points of all CPU modules: 4416 points	Section 4.1.2
	Communication using CPU shared memory by programs	----	With TO, S.TO and/or FROM instructions and instruction using the multiple CPU area device (U3En\G□).	Section 4.1.4
	Communication from Basic model QCPU to Motion CPU	----	Instructions dedicated to the Motion CPU: 5 types, Instructions dedicated to the communication between multiple CPUs: 3 types	Section 4.2, Section 4.3.1
	Communication from Basic model QCPU to PC CPU module	----	Communication dedicated instruction between multiple CPUs: 1 type	Section 4.3.2
Scan time	Factors for increasing scan time	Writing data during RUN or communication processing time setting, etc.	In addition to factors for the single CPU system, refresh processing for CPU modules in Multiple CPU system and waiting time may increase the scan time.	Section 5.2
Parameter	Parameters added for multiple CPU system	----	1) No. of CPU modules (Multiple CPU setting) 2) Control CPU (detailed I/O assignment setting) 3) Out-of-group I/O setting (Multiple CPU setting) 4) Operation mode for CPU error stop (Multiple CPU setting) 5) Auto refresh setting of CPU shared memory (Multiple CPU setting) Some parameters must be set to the same for all CPU modules while others may be different for each CPU module.	Section 6.1
Caution	When AnS/A compatible modules is mounted	AnS/A series compatible modules cannot be used.		Section 7.1

----: Not available

(2) When using the High Performance model QCPU

Table1.12 Difference from single CPU system

Item		Single CPU system	Multiple CPU system	Reference
System configuration	Maximum number of extension stages	7 stages		Section 2.1.2
	Maximum number of mountable I/O modules	65 - (No. of CPUs)*1,*2		
	Main base unit model*3	Q3□B, Q3□SB, Q3□RB, Q3□DB		
	Extension base unit model*3	Q5□B, Q6□B, QA1S6□B, QA6□B, QA6ADP+A5□B/A6□B, Q6□RB		
	Extension cable type	QC05B, QC06B, QC12B, QC30B, QC50B, QC100B		
	Overall distance of extension cable	Within 13.2 m		
	Power supply module model*3	Q6□P, Q6□SP, Q6□RP, A1S6□P, A6□P		
Available module	High Performance model QCPU	Function version A or later	Function version B or later	Section 2.3
	I/O module	Function version A or later		
	Intelligent function module	Function version A or later	Function version B or later (Function version A or later for QD62, QD62D and QD62E. No function restriction for QI60.)	
Available software	GX Developer	Version 4 or later	Version 6 or later	
	GX Configurator-AD	SW0D5C-QADU 00A or later*4	SW05D5C-QADU 20C or later*4	
	GX Configurator-DA	SW0D5C-QDAU 00A or later*4	SW05D5C-QDAU 20C or later*4	
	GX Configurator-SC	SW0D5C-QSCU 00A or later*4	SW05D5C-QSCU 20C or later*4	
	GX Configurator-CT	SW0D5C-QCTU 00A or later*4	SW05D5C-QCTU 20C or later*4	
	GX Configurator-TI	Version 1.00A or later*4		
	GX Configurator-TC	SW0D5C-QCTU 00A or later		
	GX Configurator-FL	SW0D5C-QFLU 00A or later		
	GX Configurator-QP	Version 2.00A or later		
	GX Configurator-PT	Version 1.00A or later		
	GX Configurator-AS	Version 1.13P or later		
	GX Configurator-MB	Version 1.00A or later		
	GX Configurator-DN	Version 1.00A or later		
Concept	CPU module mounting position and CPU No.	CPU slot only (no CPU No.)	CPU slot = CPU No. 1 Slot 0 = CPU No. 2 Slot 1 = CPU No. 3 Slot 2 = CPU No. 4	Section 3.1.2
	I/O number assignment	Slot 0 is 00H.	The number assigned to the right of the CPU module placed in the rightmost position in the multiple CPU setting is 00H.*5	Section 3.3.1
	Restriction on number of mountable modules	The number of mountable modules per CPU module is restricted depending on the module type.	The number of mountable modules per QCPU and per system is restricted depending on the module type.	Section 2.4

* 1: "No. of CPUs" indicates the number of CPU modules set in the "No. of PLCs" of the GX Developer.
It is 1 for the single CPU system.
* 2: When the PC CPU module is mounted on the multiple CPU system, the maximum number of mountble I/O modules is 65 - (No. of CPUs +1).
* 3: When the Motion CPU or PC CPU module is mounted on the multiple CPU system, Q3□RB, Q6□RB, and Q6□RP are not available.
* 4: For some intelligent function modules, different version may be used.
* 5: When the PC CPU module is mounted, the slot to the right of the PC CPU module is 10H.

Table1.12 Difference from single CPU system (continued)

Item		Single CPU system	Multiple CPU system	Reference
Access range	Access from CPU module to other modules	All modules can be controlled.	Setting the relations between the CPU module and other modules with the PLC parameter (control CPU) is required.	Section 3.4
	Access from GOT	Accessible	Accessible to the High Performance model QCPU of the specified CPU No.	Manuals for GOT
	Access with instruction using link direct	Accessible	Only control CPU is accessible.	Section 3.6
	Access to CC-Link	Accessible	Only control CPU is accessible.	CC-Link system master/local module manuals
	Access from peripheral devices	Accessible through USB or RS-232 cable, or via network.	Accessible through USB or RS-232 cable, or via network. For access when the Motion CPU, or PC CPU module is connected, refer to the relevant manual.	Section 2.2
Clock function	Clock data used by intelligent function module (QD75, etc.)	Clock data of the High Performance model QCPU is used.	Clock data of the High Performance model QCPU (CPU No. 1) is used.	Section 3.8
Operation	CPU module resetting operation	The entire system is reset by resetting the High Performance model QCPU.	The entire system is reset by resetting the High Performance model QCPU (CPU No. 1). (Resetting CPU No. 2 to 4 individually is not allowed.)	Section 3.9
	Operation for CPU module stop error	The system stops.	For a stop error of the High Performance model QCPU of CPU No. 1, the multiple CPU system stops. (CPU modules No. 2 to 4 are in "MULTI CPU DOWN (Error code: 7000)" status. For a stop error occurred in any of CPU No. 2 to 4, the operation depends on the parameter setting of "Operation mode".	Section 3.10
Communication between CPU modules	Communication using CPU shared memory by auto refresh	----	Up to 2k words in total of 4 settings per CPU. The total for all CPU modules is 8k words.	Section 4.1.2
	Communication using CPU shared memory by programs	----	With S.TO / FROM instructions and instruction using the multiple CPU area device (U3En\G□).	Section 4.1.4
	Communication from high performance model QCPU to Motion CPU	----	Instructions dedicated to the Motion CPU: 5 types, Instructions dedicated to the communication between multiple CPUs: 3 types	Section 4.2, Section 4.3.1
	Communication from high performance model QCPU to PC CPU module	----	Instruction dedicated to the communication between multiple CPUs: 1 type	Section 4.3.2
Scan time	Factors for increasing scan time	Writing data during RUN or communication processing time setting, etc.	In addition to factors for the single CPU system, refresh processing for CPU modules in Multiple CPU system and waiting time may increase the scan time.	Section 5.2

----: Not available

Table1.12 Difference from single CPU system (continued)

		Single CPU system	Multiple CPU system	Reference
Parameter	Parameters added for multiple CPU system	----	1) No. of CPU modules (Multiple CPU setting) 2) Control CPU (detailed I/O assignment setting) 3) Out-of-group I/O setting (Multiple CPU setting) 4) Operation mode for CPU error stop (Multiple CPU setting) 5) Auto refresh setting of CPU shared memory (Multiple CPU setting) Some parameters must be set to the same for all CPU modules while others may be different for each CPU module.	Section 6.1
Caution	When AnS/A compatible modules is mounted	Use is allowed.	Use is allowed when the High Performance model QCPU is set to the control CPU.	Section 7.1

----: Not available

(3) When using the Process CPU

Table1.13 Difference from single CPU system

Item		Single CPU system	Multiple CPU system	Reference
System configuration	Maximum number of extension stages	7 stages		Section 2.1.2
	Maximum number of mountble I/O modules	65 - (No. of CPUs)*1		
	Main base unit model*3	Q3□B, Q3□RB, Q3□DB		
	Extension base unit model*3	Q5□B, Q6□B, Q6□RB		
	Extension cable type	QC05B, QC06B, QC12B, QC30B, QC50B, QC100B		
	Overall distance of extension cable	Within 13.2 m		
	Power supply module model*3	Q6□P, Q6□RP		
Available module	Process CPU	No restrictions on function version		Section 2.3
	I/O module	Function version A or later		
	Intelligent function module	Function version A or later	Function version B or later (Function version A or later for QD62, QD62D and QD62E. No version restriction for QI60.)	
Available software	GX Developer	Version 7.10L or later		
	GX Configurator-AD	Version 1.13P or later*4		
	GX Configurator-DA	Version 1.13P or later*4		
	GX Configurator-SC	Version 1.13P or later		
	GX Configurator-CT	Version 1.13P or later*4		
	GX Configurator-TI	Version 1.13P or later*4		
	GX Configurator-TC	Version 1.13P or later		
	GX Configurator-FL	Version 1.13P or later		
	GX Configurator-QP	Version 2.13P or later		
	GX Configurator-PT	Version 1.13P or later		
	GX Configurator-AS	Version 1.13P or later		
	GX Configurator-MB	Version 1.00A or later		
	GX Configurator-DN	Version 1.13P or later		
Concept	CPU module mounting position and CPU No.	CPU slot only (no CPU No.)	CPU slot = CPU No. 1 Slot 0 = CPU No. 2 Slot 1 = CPU No. 3 Slot 2 = CPU No. 4	Section 3.1.2
	I/O number assignment	Slot 0 is 00H.	The number assigned to the right of the CPU module placed in the rightmost position in the multiple CPU setting is 00H.*5	Section 3.3.1
	Restrictions on number of mountable modules	The number of mountable modules per CPU module is restricted depending on the module type.	The number of mountable modules per CPU module and per system is restricted depending on the module type.	Section 2.4

* 1: "No. of CPUs" indicates the number of CPU modules set in the "No. of PLCs" of the GX Developer.
It is 1 for the single CPU system
* 2: When the PC CPU module is mounted on the multiple CPU system, the maximum number of mountble I/O modules is 65 - (No. of CPUs +1).
* 3: When the Motion CPU or PC CPU module is mounted on the multiple CPU system, Q3□RB, Q6□RB, and Q6□RP are not available.
* 4: For some intelligent function modules, different version may be used.
* 5: When the PC CPU module is mounted, the slot to the right of the PC CPU module is 10H.

Table1.13 Difference from single CPU system (continued)

Item		Single CPU system	Multiple CPU system	Reference
Access range	Access from CPU module to other modules	All modules can be controlled.	Setting the relations between the CPU module and other modules with the PLC parameter (control CPU) is required.	Section 3.4
	Access from GOT	Accessible	Accessible to the Process CPU of the specified CPU No.	Manuals for GOT
	Access with instruction using link direct	Accessible	Only control CPU is accessible.	Section 3.6
	Access to CC-Link	Accessible	Only control CPU is accessible.	CC-Link system master/local module manuals
	Access from peripheral devices	Accessible through USB or RS-232 cable, or via network.	Accessible through USB or RS-232 cable, or via network. When the Motion CPU or PC CPU module is connected, refer to the relevant manual for details.	Section 2.2
Clock function	Clock data used by intelligent function module (QD75, etc.)	Clock data of the Process CPU is used.	Clock data of the Process CPU (CPU No. 1) is used.	Section 3.6
Operation	CPU module resetting operation	The entire system is reset by resetting the Process CPU.	The entire system is reset by resetting the Process CPU (CPU No. 1). (Resetting CPU No. 2 to 4 individually is not allowed.)	Section 3.9
	Operation for CPU module stop error	The system stops.	For a stop error of the Process CPU of CPU No. 1, the multiple CPU system stops. (CPU modules No. 2 to 4 are in "MULTI CPU DOWN (Error code: 7000)" status. For a stop error occurred in any of CPU No. 2 to 4, the operation depends on the parameter setting of "Operation mode".	Section 3.10
Communication between CPU modules	Communication using CPU shared memory by auto refresh	----	Up to 2k words in total of 4 settings per CPU. The total for all CPU modules is 8k words.	Section 4.1.2
	Communication using CPU shared memory by programs	----	With TO / FROM instructions and instruction using the multiple CPU area device (U3En\G□).	Section 4.1.4
	Communication from Process CPU to Motion CPU	----	Instructions dedicated to the Motion CPU: 5 types, Instructions dedicated to the communication between multiple CPUs: 3 types	Section 4.2, Section 4.3.1
	Communication from Process CPU to PC CPU module	----	Communication dedicated instruction between multiple CPUs: 1 type	Section 4.3.2
Scan time	Factors for increasing scan time	Writing data during RUN or communication processing time setting, etc.	In addition to factors for the single CPU system, refresh processing for CPU modules in Multiple CPU system and waiting time may increase the scan time.	Section 5.2
Parameter	Parameters added for multiple CPU system	----	1) No. of CPU modules (Multiple CPU setting) 2) Control CPU (detailed I/O assignment setting) 3) Out-of-group I/O setting (Multiple CPU setting) 4) Operation mode for CPU error stop (Multiple CPU setting) 5) Auto refresh setting of CPU shared memory (Multiple CPU setting) Some parameters must be set to the same for all CPU modules while others may be different for each CPU module.	Section 6.1
Caution	When AnS/A compatible modules is mounted	AnS/A series compatible modules cannot be used.		Section 7.1

----: Not available

(4) When using the Universal model QCPU

Table1.14 Difference from single CPU system

Item		Single CPU system	Multiple CPU system	Reference
System configuration	Maximum number of extension stages	7 stages (when the Q02UCPU is used:4 stages)		Section 2.1.3
	Maximum number of mountble I/O modules	65 - (No. of CPUs) (when the Q02UCPU is used:37 - (No. of CPUs))*1,*2		
	Main base unit model*3	Q3□B, Q3□SB, Q3□RB, Q3□DB		
	Extension base unit model*3	Q5□B, Q6□B, Q6□RB		
	Extension cable type	QC05B, QC06B, QC12B, QC30B, QC50B, QC100B		
	Overall distance of extension cable	Within 13.2 m		
	Power supply module model*3	Q6□P, Q6□SP, Q6□RP	Q6□P	
Available module	Universal model QCPU	No restrictions on function version		Section 2.3
	I/O module	Function version A or later		
	Intelligent function module	Function version A or later	Function version B or later (Function version A or later for QD62, QD62D and QD62E. No version restriction for QI60.)	
Available software	GX Developer	Version 8.48A or later		
	GX Configurator-AD	Version 2.05F or later		
	GX Configurator-DA	Version 2.06G or later		
	GX Configurator-SC	Version 2.12N or later		
	GX Configurator-CT	Version 1.25B or later		
	GX Configurator-TI	Version 1.24A or later		
	GX Configurator-TC	Version 1.23Z or later		
	GX Configurator-FL	Version 1.23Z or later		
	GX Configurator-QP	Version 2.24A or later		
	GX Configurator-PT	Version 1.23Z or later		
	GX Configurator-AS	Version 1.22Y or later		
	GX Configurator-MB	Version 1.08J or later		
	GX Configurator-DN	Version 1.23Z or later		
Concept	CPU module mounting position and CPU No.	CPU slot only (no CPU No.)	CPU slot = CPU No. 1 Slot 0 = CPU No. 2 Slot 1 = CPU No. 3 Slot 2 = CPU No. 4*4	Section 3.1.3
	I/O number assignment	Slot 0 is 00H.	The number assigned to the right of the CPU module placed in the rightmost position in the multiple CPU setting is 00H.	Section 3.3.1
	Restrictions on number of mountable modules	The number of mountable modules per CPU module is restricted depending on the module type.	The number of mountable modules per CPU module and per system is restricted depending on the module type.	Section 2.4

* 1: "No. of CPUs" indicates the number of CPU modules set in the "No. of PLCs" of the GX Developer.
It is 1 for the single CPU system.
* 2: When the PC CPU module is mounted on the multiple CPU system, the maximum number of mountble I/O modules is 65 - (No. of CPUs +1) (when the Q02UCPU is used:37 - (No. of CPUs + 1)).
* 3: When the Motion CPU or PC CPU module is mounted on the multiple CPU system, Q3□RB, Q6□RB, and Q6□RP are not available.
* 4: When the Q02UCPU is used as the CPU module 1, up to three CPU modules can be mounted. Therefore, the CPU No. 4 does not exist.

Table1.14 Difference from single CPU system (continued)

Item		Single CPU system	Multiple CPU system	Reference
Access range	Access from CPU module to other modules	All modules can be controlled.	Setting the relations between the CPU module and other modules with the PLC parameter (control CPU) is required.	Section 3.4
	Access from GOT	Accessible	Accessible to the Universal model QCPU of the specified CPU No.	Manuals for GOT
	Access with instruction using link direct	Accessible	Only control CPU is accessible.	Section 3.6
	Access to CC-Link	Accessible	Only control CPU is accessible.	CC-Link system master/local module manuals
	Access from peripheral devices	Accessible through USB or RS-232 cable, or via network.	Accessible through USB or RS-232 cable, or via network. For access when the Motion CPU or PC CPU module is connected, refer to the relevant manual.	Section 2.2
Clock function	Clock data used by CPU modules No.2 to No.4	----	Clock data of the Universal model QCPU (CPU No.1) is used.*5	Section 3.8.1
	Clock data used by intelligent function module (QD75, etc.)	Clock data of the Universal model QCPU is used.	Clock data of the Universal model QCPU (CPU No. 1) is used.	Section 3.8.2
Operation	CPU module resetting operation	The entire system is reset by resetting the Universal model QCPU.	The entire system is reset by resetting the Universal model QCPU (CPU No. 1). (Resetting CPU No. 2 to 4 individually is not allowed.)	Section 3.9
	Operation for CPU module stop error	The system stops.	For a stop error of the Universal model QCPU of CPU No. 1, the multiple CPU system stops. (CPU modules No. 2 to 4 are in "MULTI CPU DOWN (Error code: 7000)" status. For a stop error occurred in any of CPU No. 2 to 4, the operation depends on the parameter setting of "Operation mode".	Section 3.10
	Multiple CPU system synchronized boot-up	----	It is possible to choose whether to synchronize the boot-up of CPU modules in the Multiple CPU system or not. (The default synchronizes the boot-up of all CPU modules.)	Section 4.5
Communication between CPU modules	Communication by auto refresh using QCPU standard memory	----	Memory size which can be used by all CPU modules is as follows: • When 2 CPU modules are used: 14k words • When 3 CPU modules are used: 13k words • When 4 CPU modules are used: 12k words	Section 4.1.3
	Communication by auto refresh using multiple CPU high speed transmission area*6	----	With TO / FROM instructions and instruction using the multiple CPU area device (U3En\G□).	Section 4.1.4
	Communication from Universal model QCPU to Motion CPU	----	Instructions dedicated to the Motion CPU: 5 types, Instructions dedicated to the communication between multiple CPUs: 3 types	Section 4.2, Section 4.3.1
Scan time	Factors for increasing scan time	Writing data during RUN or communication processing time setting, etc.	In addition to factors for the single CPU system, refresh processing for CPU modules in Multiple CPU system and waiting time may increase the scan time.	Section 5.2

----: Not available

* 5: When a Universal model QCPU (except Q02UCPU) or Motion CPU (Q172DCPU or Q173DCPU) is used as any of CPUs No.2 to No.4, clock data in CPU No.1 can be used.
* 6: When CPU No.1 is the Q02UCPU, the communication by the auto refresh using the multiple CPU high speed transmission area is not available.

Table1.14 Difference from single CPU system (continued)

Item		Single CPU system	Multiple CPU system	Reference
Parameter	Parameters added for multiple CPU system	----	1) No. of CPU modules (Multiple CPU setting) 2) Control CPU (detailed I/O assignment setting) 3) Out-of-group I/O setting (Multiple CPU setting) 4) Operation mode for CPU error stop (Multiple CPU setting) 5) Multiple CPU synchronized boot-up (Multiple CPU settings) 6) Multiple CPU high speed transmission area setting (Multiple CPU settings)*7 7) Communication area setting(refresh setting) Some parameters must be set to the same for all CPU modules while others may be different for each CPU module.	Section 6.1
Caution	When AnS/A compatible modules is mounted	AnS/A series compatible modules cannot be used.		Section 7.1

----: Not available

* 7: When CPU No.1 is the Q02UCPU, the multiple CPU high speed transmission area cannot be set up.

CHAPTER2 SYSTEM CONFIGURATION

This chapter explains the system configuration of Multiple CPU Systems, and the precautions for Multiple CPU System configuration.

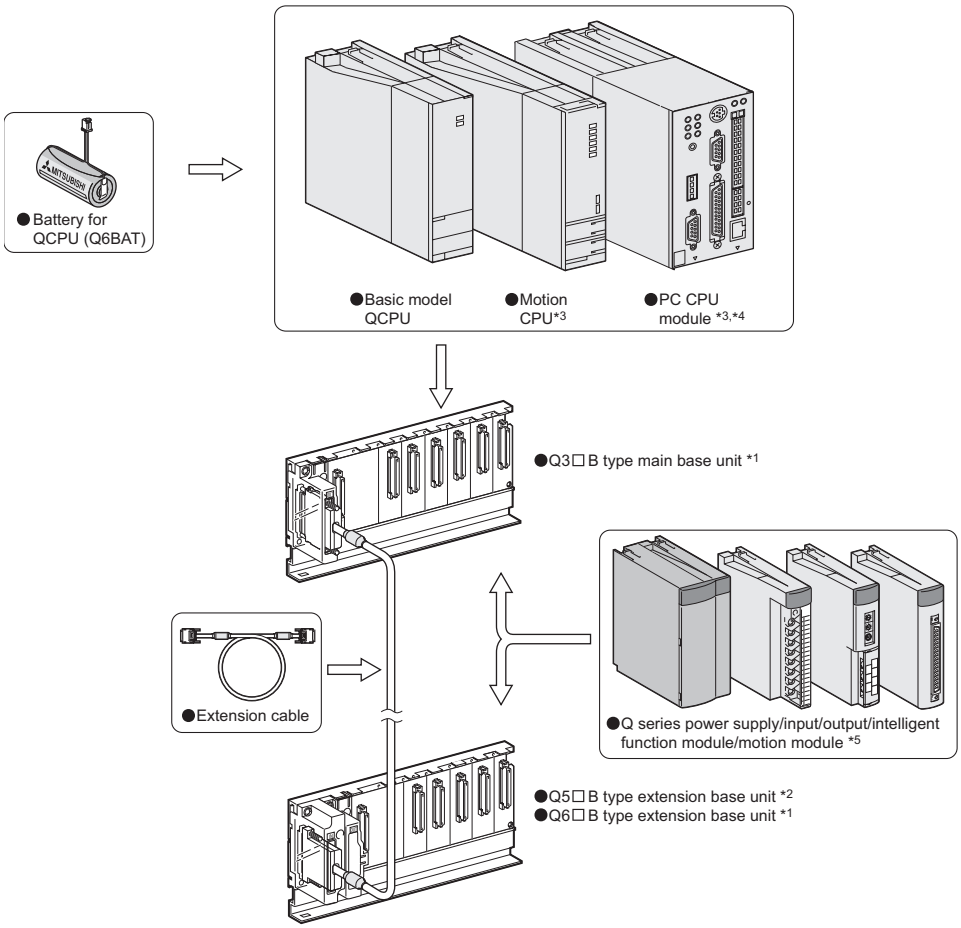
2.1 System configuration

2.1.1 System configuration using Basic model QCPU (Q00CPU, Q01CPU)

This following explains the system configuration using the Basic model QCPU.

(1) System using the main base unit (Q3□B)

(a) System configuration



* 1: As a power supply module, use the Q series power supply module.
  Make the power consumption within the rated output current value of the power supply module.
  The Slim type power supply module and Redundant power supply module cannot be used as a power supply module.
* 2: No Q series power supply module is required for the Q5□B type extension base unit.
* 3: The QCPU battery (Q6BAT) cannot be installed to the Motion CPU and the PC CPU module.
* 4: For further information on PC CPU module, consult CONTEC Co., Ltd
  Tel: +81-6-6472-7130
* 5: Be sure to set the control CPU of motion modules to the Motion CPU

Diagram 2.1 System configuration when Basic model QCPU is used

POINT

(1) The Q00JCPU is not available for the multiple CPU system.

(2) When the multiple CPU system is configured using the Basic model QCPU as the CPU No.1, only the following CPU modules can be used as the CPUs No.2 and 3.

- Motion CPU(Q172CPUN,Q173CPUN,Q172HCPU,Q173HCPU)
- PC CPU module

(b) Outline of system configuration

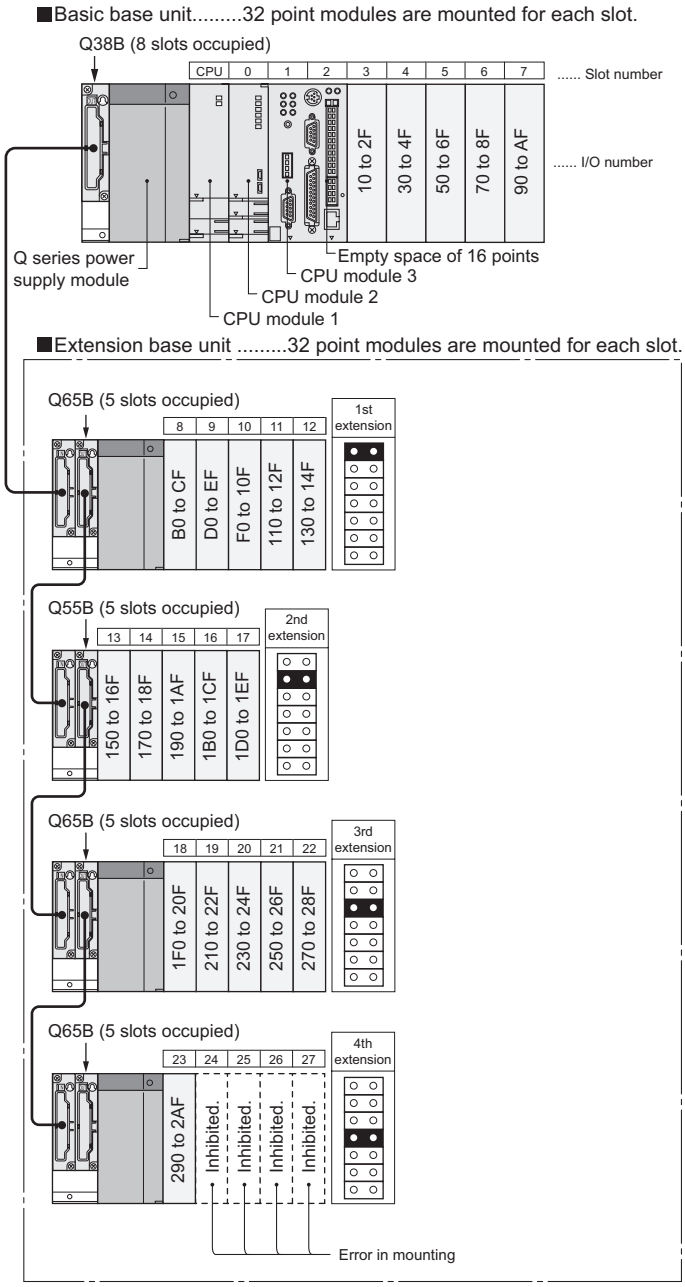


Diagram 2.2 System configuration example for using Basic model QCPU

Table2.1 Restrictions on System Configuration, Applicable Base Units, Extension Cables, Power Supply Modules

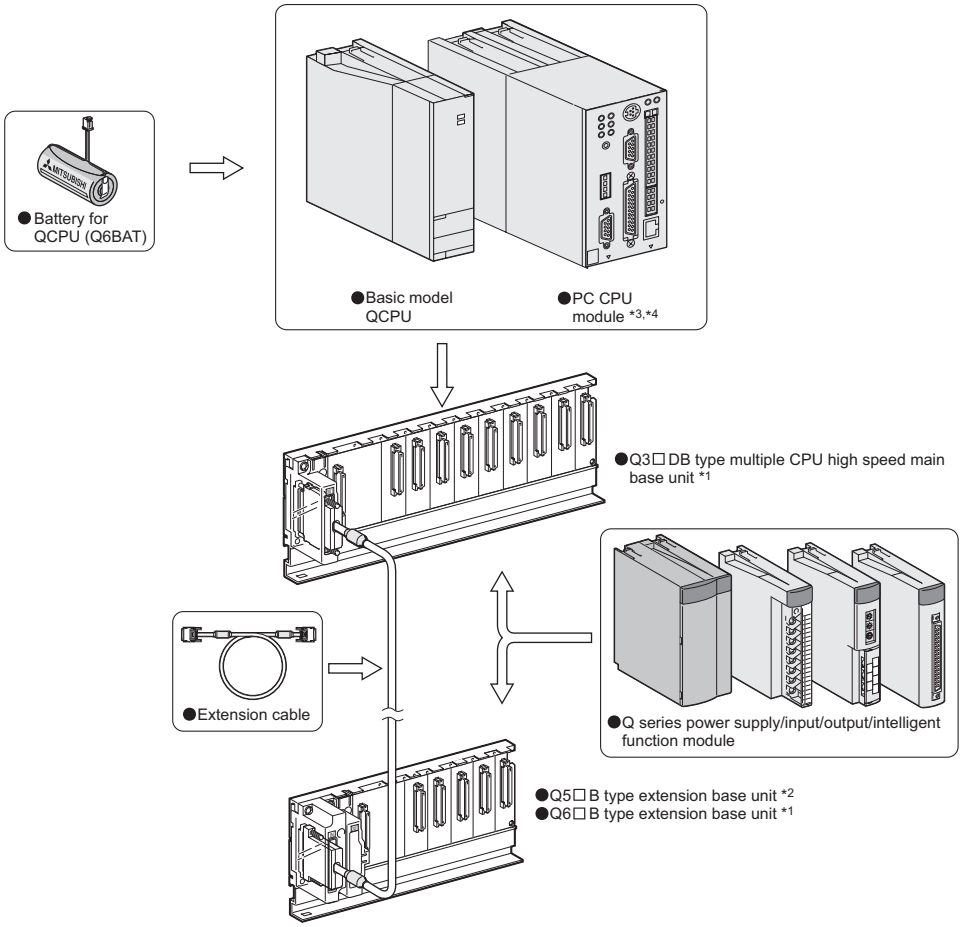
CPU number	CPU1: CPU No. 1 (Basic model QCPU), CPU2: CPU No. 2 (Motion CPU), CPU3: CPU No. 3 (PC CPU module)	
Maximum number of extension stages	4 extension units	
Maximum number of mountble I/O modules	25 - (No. of CPUs)	
Available main base unit model	Q33B, Q35B, Q38B, Q312B	
Available extension base unit model	Model not requiring power supply module	Q52B, Q55B
	Model requiring Q series power supply module	Q63B, Q65B, Q68B, Q612B
Available extension cable type	QC05B, QC06B, QC12B, QC30B, QC50B, QC100B	
Available power supply module model	Q61P-A1, Q61P-A2, Q61P, Q62P, Q63P, Q64P	

Precautions

- Do not use an extension cable longer than 13.2m (43.31 ft).
- When using an extension cable, keep it away from the main circuit (high voltage and large current) line.
- Set the number of extension stages so as not to be duplicated.
- The QA1S6□B, QA6□B, QA6ADP+A5□B/A6□B, or Q6R□B cannot be connected as an extension base unit.
- Although there is no restriction on the connection order of the Q5□B and the Q6□B, check the availability of them by referring to QCPU User's Manual (Hardware Design, Maintenance and Inspection) when both the Q5□B and the Q6□B exist as the extension base unit.
- Connect the OUT connector of an extension base unit and the IN connector of the adjacent extension base unit by an extension cable.
- When 26 modules or more are mounted, an error "SP. UNIT LAY ERR." (error code: 2124) occurs. (The number of mountable modules includes one CPU module.)
- The redundant base unit cannot be used when the Basic model QCPU is mounted on the multiple CPU system.
- "No. of CPUs" is the number of CPUs set by [No. of PLC] of GX Developer.
- The PC CPU module occupies two slots. Therefore, when the PC CPU module is used, the maximum number of I/O modules is decreased by 1 from the value indicated in Table 2.1.
- For details of the Motion CPU, and PC CPU module, refer to the manual of each CPU module.

(2) When using the Multiple CPU High speed main base unit (Q3□DB)

(a) System configuration



* 1: As a power supply module, use the Q series power supply module.
  Make the power consumption within the rated output current value of the power supply module.
  The Slim type power supply module and Redundant power supply module cannot be used as a power supply module.
* 2: No Q series power supply module is required for the Q5□B type extension base unit.
* 3: The QCPU battery (Q6BAT) cannot be installed to the PC CPU module.
* 4: For further information on PC CPU module, consult CONTEC Co., Ltd
  Tel: +81-6-6472-7130

Diagram 2.3 System configuration when Basic model QCPU is used

POINT

(1) The Q00JCPU is not available for the multiple CPU system.

(2) When the multiple CPU system is configured using the Basic model QCPU as the CPU No.1, only the following CPU modules can be used as the CPUs No.2.

- PC CPU module

(b) Outline of system configuration

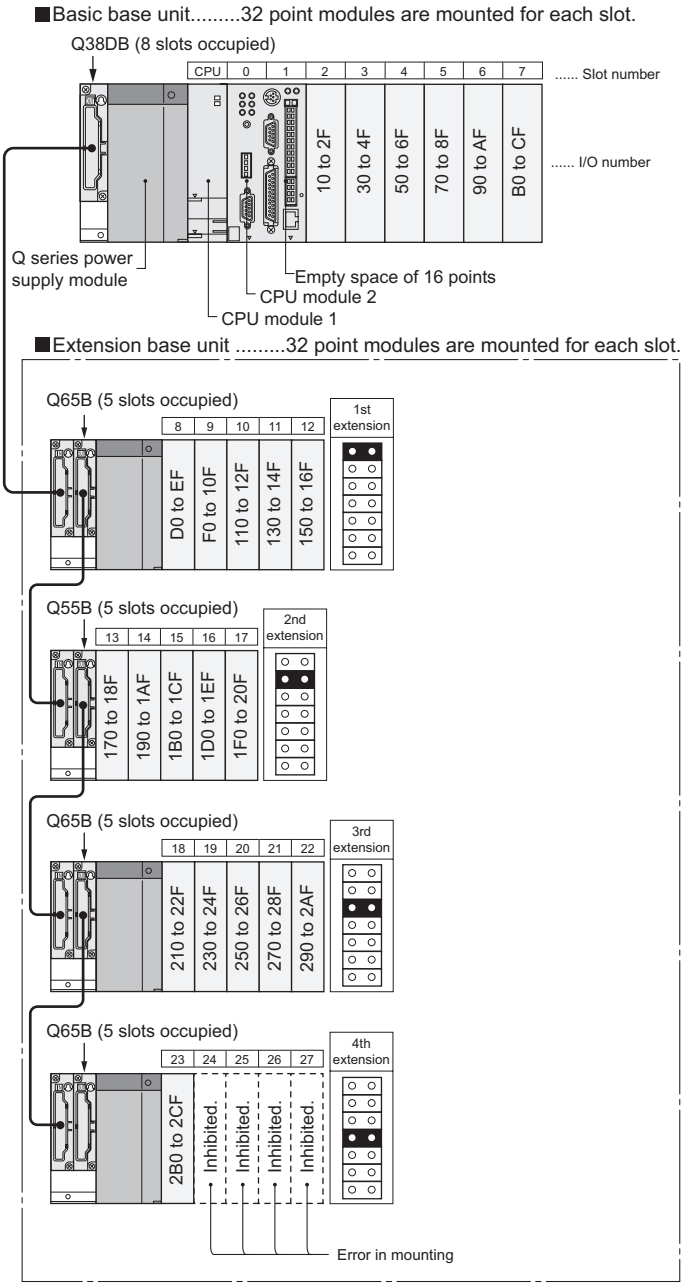


Diagram 2.4 System configuration example for using Basic model QCPU

Table2.2 Restrictions on System Configuration, Applicable Base Units, Extension Cables, Power Supply Modules

CPU number	CPU1: CPU No. 1 (Basic model QCPU), CPU2: CPU No. 2 (PC CPU module)	
Maximum number of extension stages	4 extension units	
Maximum number of mountble I/O modules	25 - (No. of CPUs)	
Available main base unit model	Q33B, Q35B, Q38B, Q312B	
Available extension base unit model	Model not requiring power supply module	Q52B, Q55B
	Model requiring Q series power supply module	Q63B, Q65B, Q68B, Q612B
Available extension cable type	QC05B, QC06B, QC12B, QC30B, QC50B, QC100B	
Available power supply module model	Q61P-A1, Q61P-A2, Q61P, Q62P, Q63P, Q64P	

Precautions

- Do not use an extension cable longer than 13.2m (43.31 ft).
- When using an extension cable, keep it away from the main circuit (high voltage and large current) line.
- Set the number of extension stages so as not to be duplicated.
- The QA1S6□B, QA6□B, QA6ADP+A5□B/A6□B, or Q6R□B cannot be connected as an extension base unit.
- Although there is no restriction on the connection order of the Q5□B and the Q6□B, check the availability of them by referring to QCPU User's Manual (Hardware Design, Maintenance and Inspection) when both the Q5□B and the Q6□B exist as the extension base unit.
- Connect the OUT connector of an extension base unit and the IN connector of the adjacent extension base unit by an extension cable.
- When 26 modules or more are mounted, an error "SP. UNIT LAY ERR." (error code: 2124) occurs. (The number of mountable modules includes one CPU module.)
- The redundant base unit cannot be used when the Basic model QCPU is mounted on the multiple CPU system.
- "No. of CPUs" is the number of CPUs set by [No. of PLC] of GX Developer.
- The PC CPU module occupies two slots. Therefore, when the PC CPU module is used, the maximum number of I/O modules is decreased by 1 from the value indicated in Table 2.1.
- For details of the PC CPU module, refer to the manual of PC CPU module.

2.1.2 System configuration using High Performance model QCPU or Process CPU as CPU No.1

This following explains the system configuration using the High Performance model QCPU and the Process CPU as the CPU No.1.

(1) When using the main base unit (Q3□B)

(a) System configuration

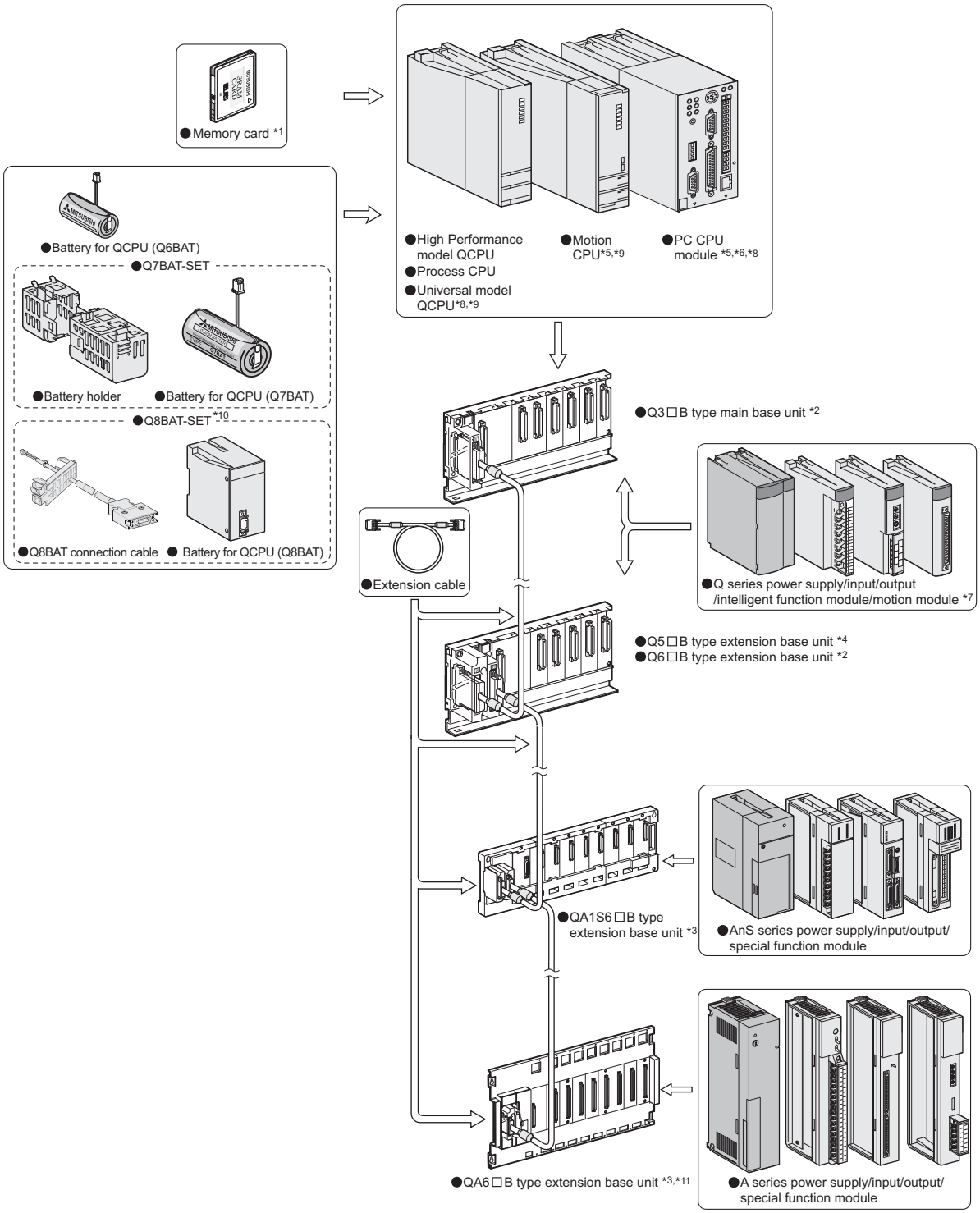


Diagram 2.5 System configuration when Q3□B is used

* 1: Only one memory card can be mounted. Select an appropriate memory card from the SRAM, Flash and ATA in accordance with application and capacity.
When a commercial memory card is used, the operation is not guaranteed.
* 2: Use the Q series power supply module for the power supply module. Keep the current consumption within the rated output current of the power supply module. The Slim power supply module and Redundant power supply module are not available for the power supply module.
* 3: When the High Performance model QCPU is set to the control CPU of the AnS/A series module, extension is allowed.
When the Process CPU or the Universal model QCPU is used, extension is not allowed.
The QA1S6□B, QA6□B, or QA6ADP+A5□B/A6□B is available for the AnS/A series compatible power supply module, the I/O module and the special function module.
* 4: The Q Series power supply module is not required for the Q5□B extension base unit.
* 5: The motion CPU and PC CPU module do not accept battery for QCPU and memory card.
* 6: For further information on PC CPU module, consult CONTEC Co., Ltd Tel: +81-6-6472-7130
* 7: Be sure to set the control CPU of the motion module to the Motion CPU.
* 8: When mounting the Universal model QCPU and the PC CPU module at the same time, use the PPC-CPU852 (MS)-512 as the PC CPU module.
* 9: The Q02UCPU cannot be mounted.
The Universal model QCPU (except Q02UCPU) and the Motion CPU (Q172CPUN, Q173CPUN, Q172HCPU, and Q173HCPU) cannot be mounted at the same time.
* 10: When the Q8BAT is used for the Universal model QCPU, use the connection cable whose connector part displays "A".
For details of connector part of a connection cable, refer to the following manual.
☞ QCPU User's Manual (Hardware Design, Maintenance and Inspection)
* 11: The QA6ADP+A5□B/A6□B is available. However, when using the QA1S6□B, the QA6ADP+A5□B/A6□B cannot be connected.

POINT

When the multiple CPU system is configured using the High Performance model QCPU or the Process CPU as the CPU No.1, only the following CPU modules can be used as the CPUs No.2 to No.4.

- High Performance model QCPU
- Process CPU
- Universal model QCPU (except Q02UCPU)
- Motion CPU(Q172CPUN0,Q173CPUN,Q172HCPU,Q173HCPU)
- PC CPU module

Note that the multiple CPU system cannot be configured using the following combinations.

- Combination of the Universal model QCPU (except Q02UCPU) and the Motion CPU (Q172CPUN, Q173CPUN, Q172HCPU, Q173HCPU)
- Combination of the Universal model QCPU (except Q02UCPU) and the PC CPU module (PPC-CPU686(MS)-64, PPC-CPU686(MS)-128)

(b) Outline of system configuration

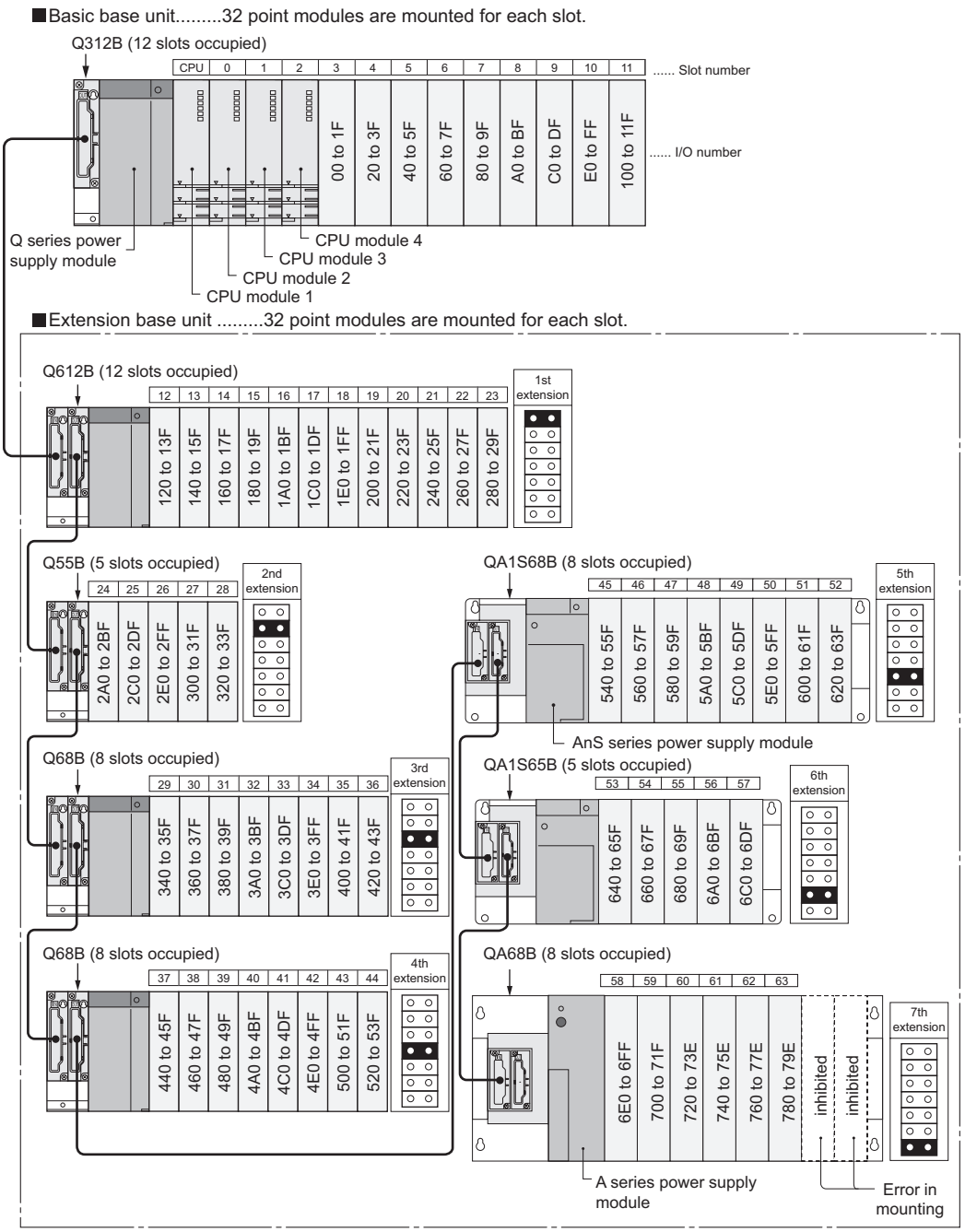


Diagram 2.6 System configuration example for using Q3□B

Table2.3 Restrictions on System Configuration, Applicable Base Units, Extension Cables, Power Supply Modules

CPU number	CPU module1: CPU No.1, CPU module 2: CPU No.2, CPU module 3: CPU No.3, CPU module 4: CPU No.4	
Maximum number of extension stages	7 extension stages	
Maximum number of mountble I/O modules	65 - (No. of CPUs)	
Available main base unit model	Q33B, Q35B, Q38B, Q312B	
Available extension base unit model	Type not requiring power supply module	Q52B, Q55B, QA6ADP+A5□B
	Type requiring Q series power supply module	Q63B, Q65B, Q68B, Q612B
	Type requiring AnS series power supply module	QA1S65B, QA1S68B
	Type requiring A series power supply module	QA65B, QA68B, QA6ADP+A6□B
Available extension cable type	QC05B, QC06B, QC12B, QC30B, QC50B, QC100B	
Available power supply module model	Q series power supply module	Q61P-A1, Q61P-A2, Q61P, Q62P, Q63P, Q64P
	AnS series power supply module	A1S61PN, A1S62PN, A1S63P
	A series power supply module	A61P, A61PN, A62P, A63P, A61PEU, A62PEU

Precautions

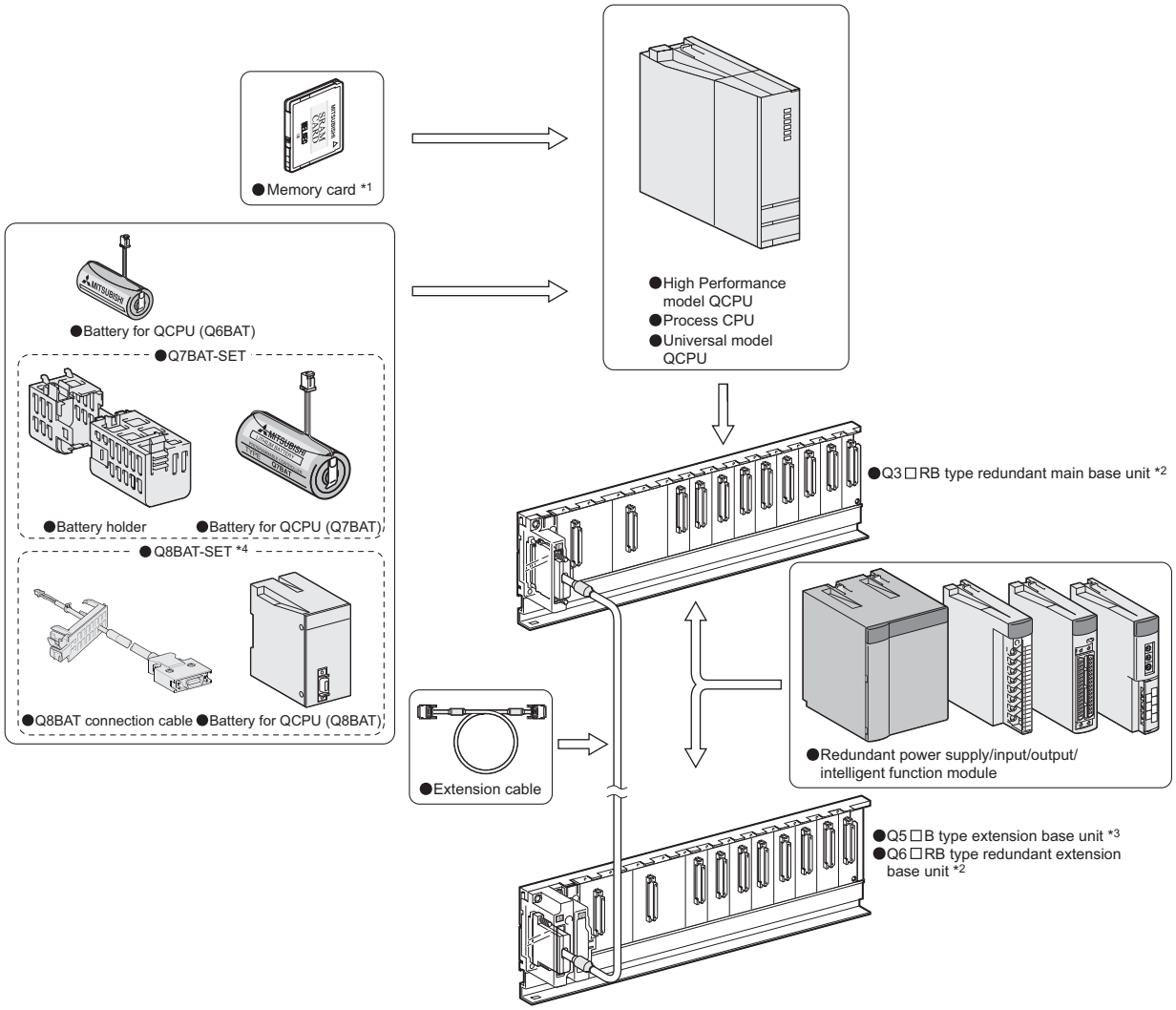
- Do not use an extension cable longer than 13.2m (43.31 ft).
- When using an extension cable, keep it away from the main circuit (high voltage and large current) line.
- Set the number of extension stages so as not to be duplicated.
- When the Q5□B, Q6□B, QA1S6□B, QA6□B, and QA6ADP+A5B/A6□B[*1] are used together as the extension base unit, mount the Q5□B/Q6□B, QA1S6□B, QA6□B, and QA6ADP+A5□B/A6□B in order from the nearest position of the main base unit.
  Although there is no restriction on the connection order of the Q5□B and the Q6□RB, check the availability of them by referring to QCPU User's Manual (Hardware Design, Maintenance and Inspection).
- The extension base units QA1S6□B, QA6□B, and QA6ADP+A5□B/A6□B can be extended when the High Performance model QCPU is set as the control CPU of the AnS/A series.
  When the Process CPU or the Universal model QCPU is used, extension is not allowed.
- The Q6□RB cannot be connected as an extension base unit.
- Connect the OUT connector of an extension base unit and the IN connector of the adjacent extension base unit by an extension cable.
- When 66 modules or more are mounted, an error "SP. UNIT LAY ERR." (error code: 2124) occurs. (The number of mountable modules includes one CPU module.)

* 1: When using the QA1S6□B, the QA6ADP+A5□B/A6□B cannot be connected.

- "No. of CPUs" is the number of CPUs set by [No. of PLC] of GX Developer.
- When mounting the Universal model QCPU (except the Q02UCPU) and the Motion CPU at the same time, use the Q172DCPU or Q173DCPU as the Motion CPU.
- When mounting the Universal model QCPU and the PC CPU module at the same time, use the PPC-CPU852 (MS)-512 as the PC CPU module.
- The PC CPU module occupies two slots. Therefore, when the PC CPU module is used, the maximum number of I/O modules is decreased by 1 from the value indicated in Table 2.3.
- For details of the Motion CPU, and PC CPU module, refer to the manual of each CPU module.

(2) When using the redundant main base unit (Q3□RB)

(a) System configuration



* 1: Only one memory card can be mounted. Select an appropriate memory card from the SRAM, Flash and ATA in accordance with application and capacity.
When a commercial memory card is used, the operation is not guaranteed.
* 2: Use the redundant power supply module for the power supply module.
The redundant power supply modules Q63RP and Q64RP can be used on one redundant power supply base unit at the same time.
The Q series power supply module and the slim type power supply module are not available for the power supply module.
* 3: The Q Series power supply module is not required for the Q5□B extension base unit.
* 4: When the Q8BAT is used for the Universal model QCPU, use the connection cable whose connector part displays "A".
For details of connector part of a connection cable, refer to the following manual.
☞ QCPU User's Manual (Hardware Design, Maintenance and Inspection)

Diagram 2.7 System configuration when Q□RB is used

POINT

(1) When the multiple CPU system is configured using the High Performance model QCPU or the Process CPU as the CPU No.1, only the following modules can be used as the CPUs No.2 to CPU No.4.
- High Performance model QCPU
- Process CPU
- Universal model QCPU (except Q02UCPU)

(2) When duplicating power supply, use the redundant power supply base unit and the redundant power supply module.
For the power supply module mounted on the redundant power supply base unit, only the redundant power supply module can be used.

(b) Outline of system configuration

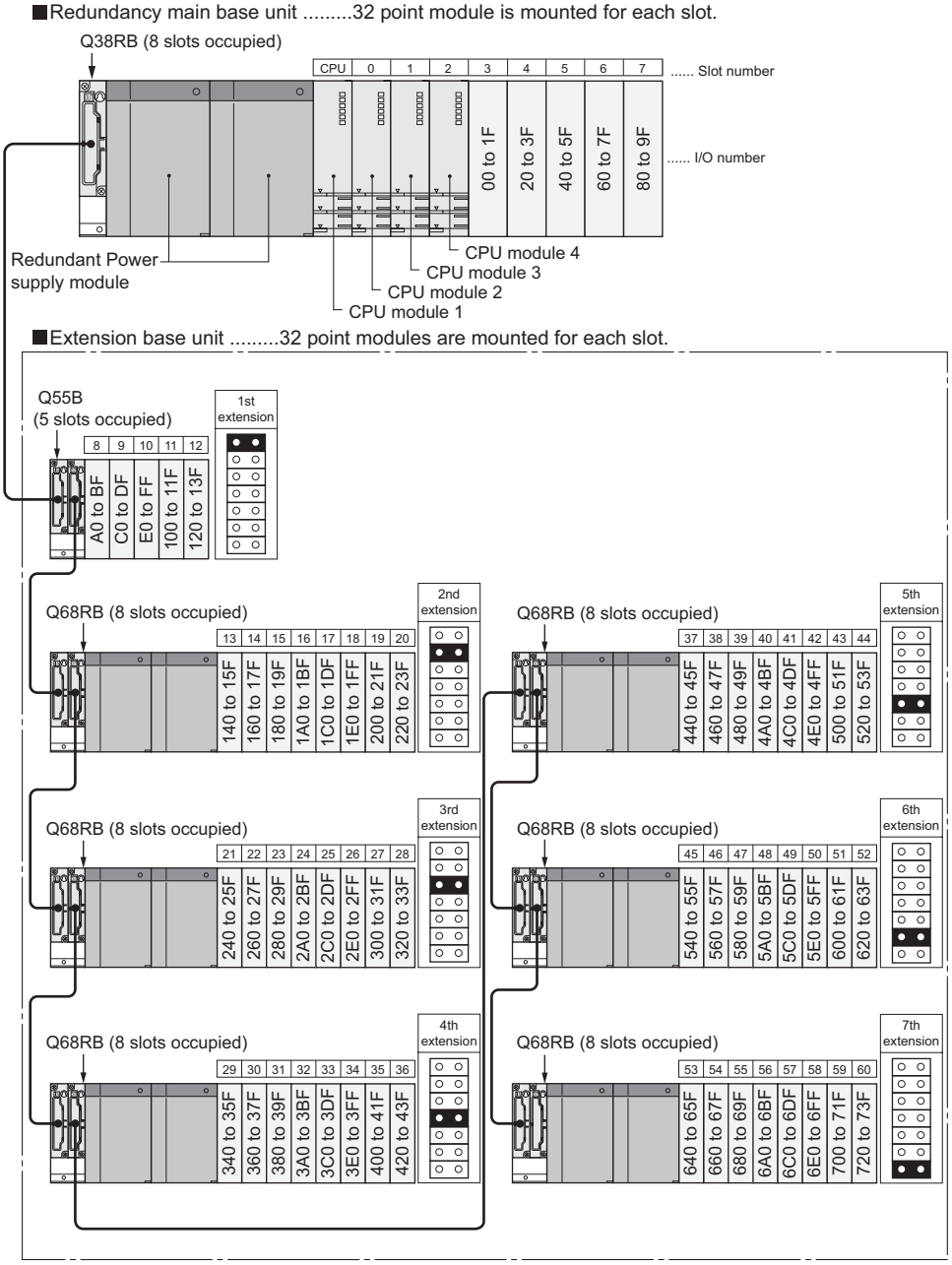


Diagram 2.8 System configuration example for using Q3□RB

Table2.4 Restrictions on System Configuration, Applicable Base Units, Extension Cables, Power Supply Modules

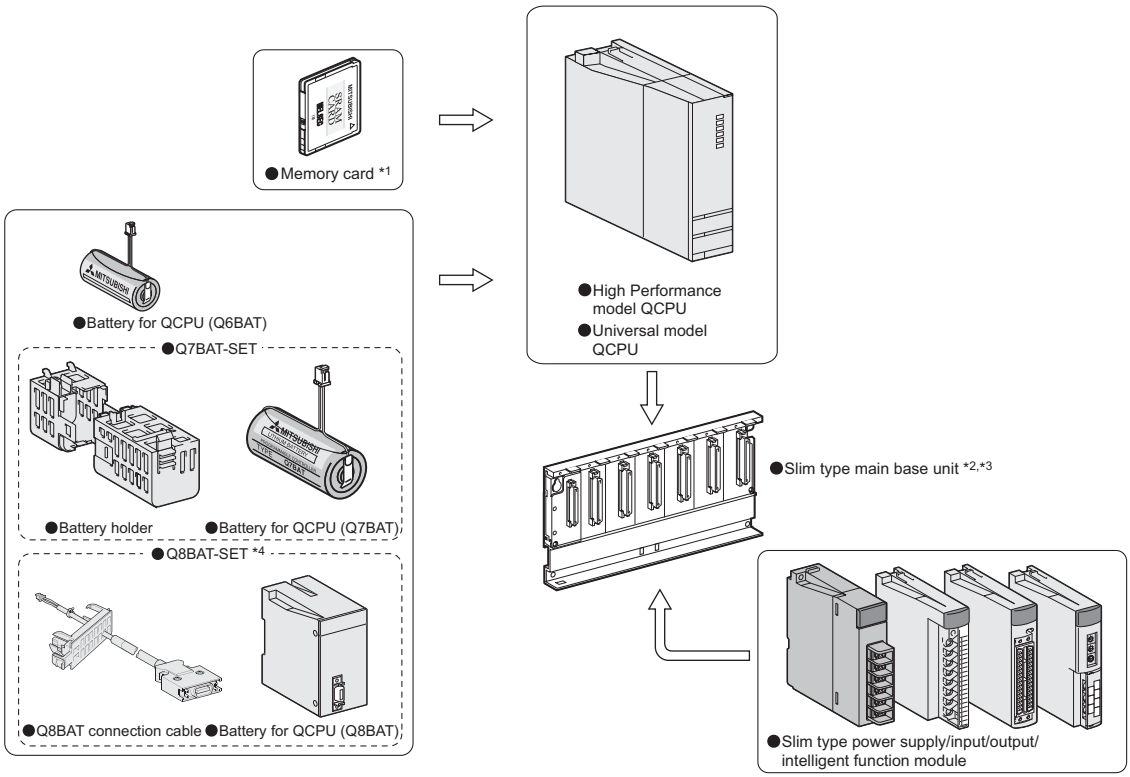
CPU number	CPU module1: CPU No.1, CPU module 2: CPU No.2, CPU module 3: CPU No.3, CPU module 4: CPU No.4	
Maximum number of extension stages	7 extension stages	
Maximum number of mounted I/O modules	65 - (No. of CPUs)	
Available main base unit model	Q38RB	
Available extension base unit model	Type not requiring power supply module	Q52B, Q55B
	Type requiring redundant power supply module	Q68RB
Available extension cable type	QC05B, QC06B, QC12B, QC30B, QC50B, QC100B	
Available power supply module model	Q63RP, Q64RP	

Precautions

- Do not use an extension cable longer than 13.2m (43.31 ft).
- When using an extension cable, keep it away from the main circuit (high voltage and large current) line.
- Set the number of extension stages so as not to be duplicated.
- Although there is no restriction on the connection order of the Q5□B and the Q6R□B, check the availability of them by referring to QCPU User's Manual (Hardware Design, Maintenance and Inspection).
- The Q6□B, QA1S6□B, QA6□B, or QA6ADP+A5□B/A6□B cannot be connected as an extension base unit.
- Connect the OUT connector of an extension base unit and the IN connector of the adjacent extension base unit by an extension cable.
- When 66 modules or more are mounted, an error "SP. UNIT LAY ERR." (error code: 2124) occurs. (The number of mountable modules includes one CPU module.)
- "No. of CPUs" is the number of CPUs set by [No. of PLC] of GX Developer.
- When the redundant base unit is used, bus connection is not available for the GOT.
- When the redundant power main base unit is used, the Motion CPU, and PC CPU module cannot be used.

(3) When using the slim type main base unit (Q3□SB)

(a) System configuration



* 1: One memory card is installed. Select an appropriate memory card from the SRAM, Flash and ATA cards according to the application and capacity.
When the memory card is used, operation is not guaranteed.
* 2: The slim type main base unit does not have an extension cable connector.
The extension base or GOT cannot be connected.
* 3: As a power supply module, use the slim type power supply module.
Keep the current consumption within the rated output current of the power supply module.
The Q series power supply module and the redundant power supply module are not available for the power supply module.
* 4: When the Q8BAT is used for the Universal model QCPU, use the connection cable whose connector part displays "A".
For details of connector part of a connection cable, refer to the following manual.
☞ QCPU User's Manual (Hardware Design, Maintenance and Inspection)

Diagram 2.9 System configuration when Q3□SB is used

POINT

When the multiple CPU system is configured using the High Performance model QCPU as the CPU No.1, only the following CPU modules can be used as the CPUs No.2 and 3.

- High Performance model QCPU
- Universal model QCPU (except Q02UCPU)

(b) Outline of system configuration

■Slim type main base unit .....32 point module is mounted for each slot.

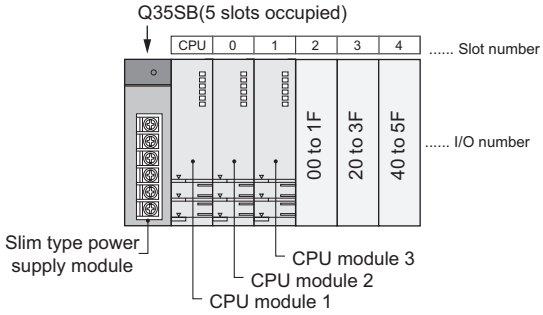


Diagram 2.10 System configuration example for using Q3□SB

Table2.5 Restrictions on System Configuration, Applicable Base Units, Extension Cables, Power Supply Modules

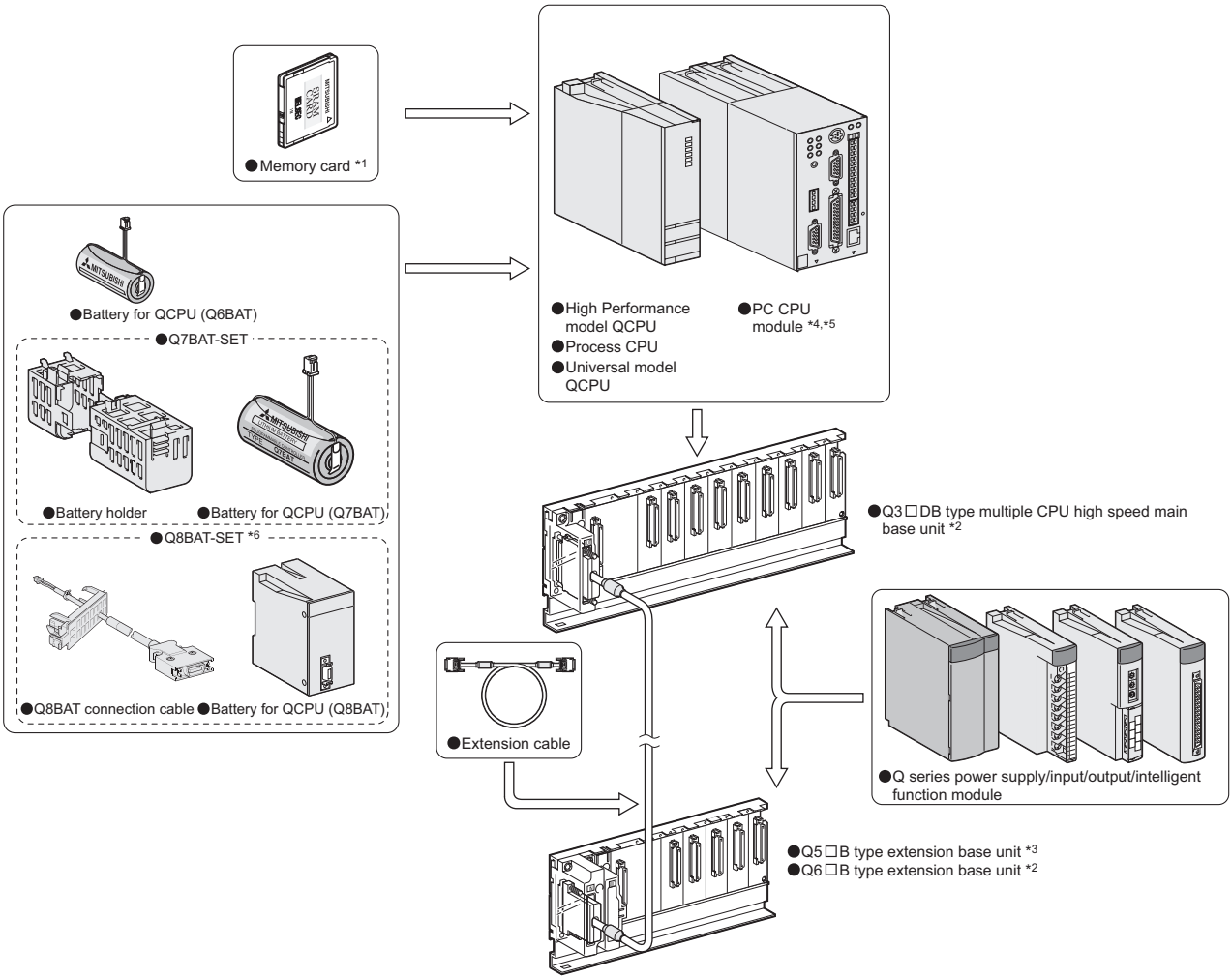
CPU number	CPU module 1: CPU No.1, CPU module 2: CPU No.2, CPU module 3: CPU No.3	
Maximum number of extension stages	Extension not allowed	
Maximum number of mountble I/O modules	Q32SB	3 - (No. of CPUs)
	Q33SB	4 - (No. of CPUs)
	Q35SB	6 - (No. of CPUs)
Available main base unit model	Q32SB, Q33SB, Q35SB	
Available power supply module model	Q61SP	

Precautions

- The slim type main base unit has no extension cable connector. The extension base or GOT cannot be connected.
- Since the current consumption of the CPU module exceeds the rated output current of the power supply module (Q61SP), mounting 4 CPU modules is not allowed.
- "No. of CPUs" indicates the number of CPU modules set in the "No. of PLCs" of the GX Developer.

(4) When using the Multiple CPU high speed main base unit (Q3□DB)

(a) System configuration



* 1: Only one memory card can be mounted. Select an appropriate memory card from the SRAM, Flash and ATA in accordance with application and capacity.
When a commercial memory card is used, the operation is not guaranteed.
* 2: Use the Q series power supply module for the power supply module. Keep the current consumption within the rated output current of the power supply module. The Slim power supply module and Redundant power supply module are not available for the power supply module.
* 3: The Q Series power supply module is not required for the Q5□B extension base unit.
* 4: The PC CPU module do not accept battery for QCPU and memory card.
* 5: For further information on PC CPU module, consult CONTEC Co., Ltd Tel: +81-6-6472-7130
* 6: When the Q8BAT is used for the Universal model QCPU, use the connection cable whose connector part displays "A".
For details of connector part of a connection cable, refer to the following manual.
☞ QCPU User's Manual (Hardware Design, Maintenance and Inspection).

Diagram 2.11 System configuration when Q3□DB is used

POINT

When the multiple CPU system is configured using the High Performance model QCPU or the Process CPU as the CPU No.1, only the following CPU modules can be used as the CPUs No.2 to No.4.

- High Performance model QCPU
- Process CPU
- Universal model QCPU (except Q02UCPU)
- PC CPU module

Note that the universal model QCPU and the PC CPU module (PPC-CPU686(MS)-64,PPC-CPU686(MS)-128) cannot be mounted at the same time.

(b) Outline of system configuration

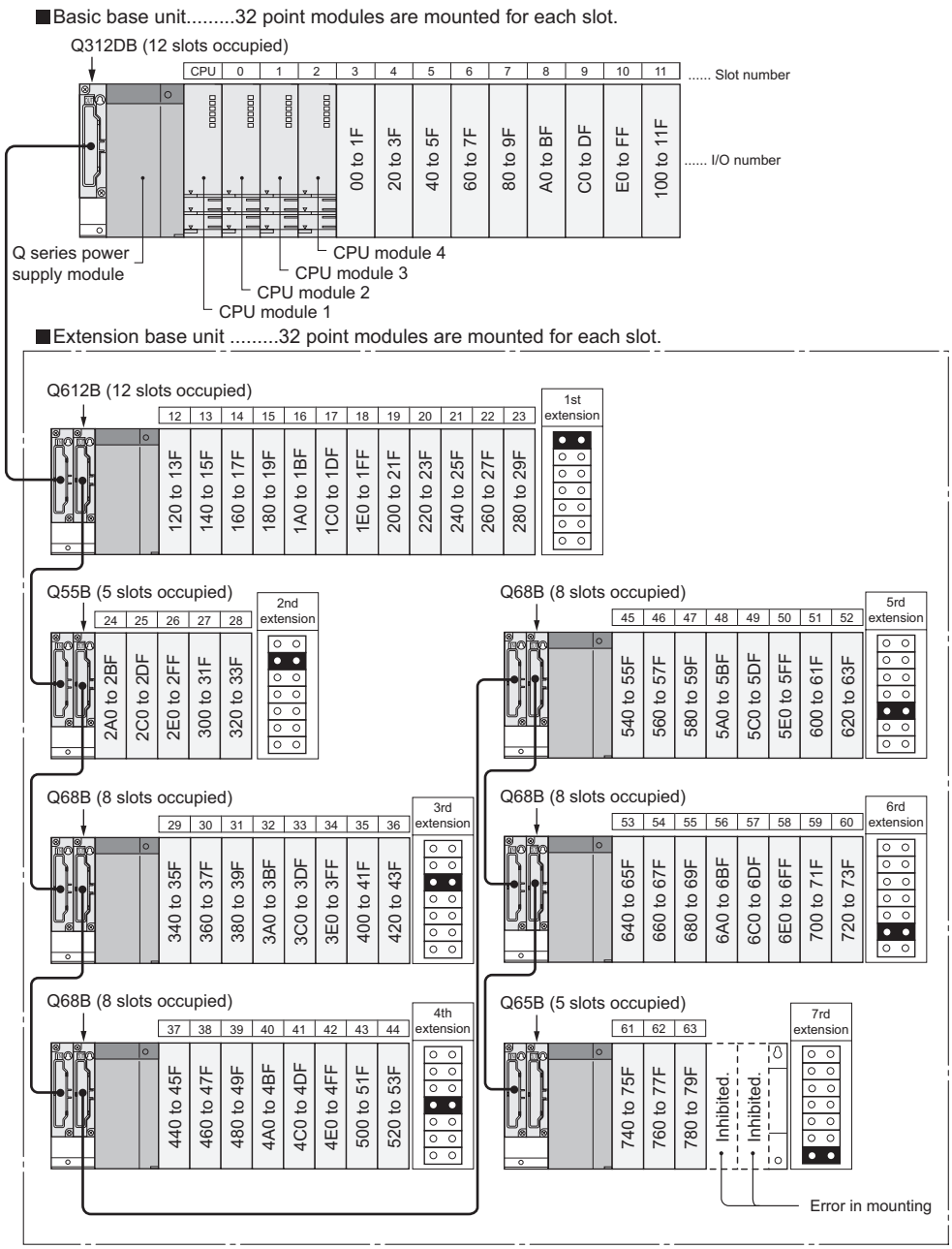


Diagram 2.12 System configuration example for using Q3□DB

Table2.6 Restrictions on System Configuration, Applicable Base Units, Extension Cables, Power Supply Modules

CPU number	CPU module1: CPU No.1, CPU module 2: CPU No.2, CPU module 3: CPU No.3, CPU module 4: CPU No.4	
Maximum number of extension stages	7 extension stages	
Maximum number of mountble I/O modules	65 - (No. of CPUs)	
Available main base unit model	Q38DB, Q312DB	
Available extension base unit model	Type not requiring power supply module	Q52B, Q55B
	Type requiring Q series power supply module	Q63B, Q65B, Q68B, Q612B
Available extension cable type	QC05B, QC06B, QC12B, QC30B, QC50B, QC100B	
Available power supply module model	Q61P-A1, Q61P-A2, Q61P, Q62P, Q63P, Q64P	

Precautions

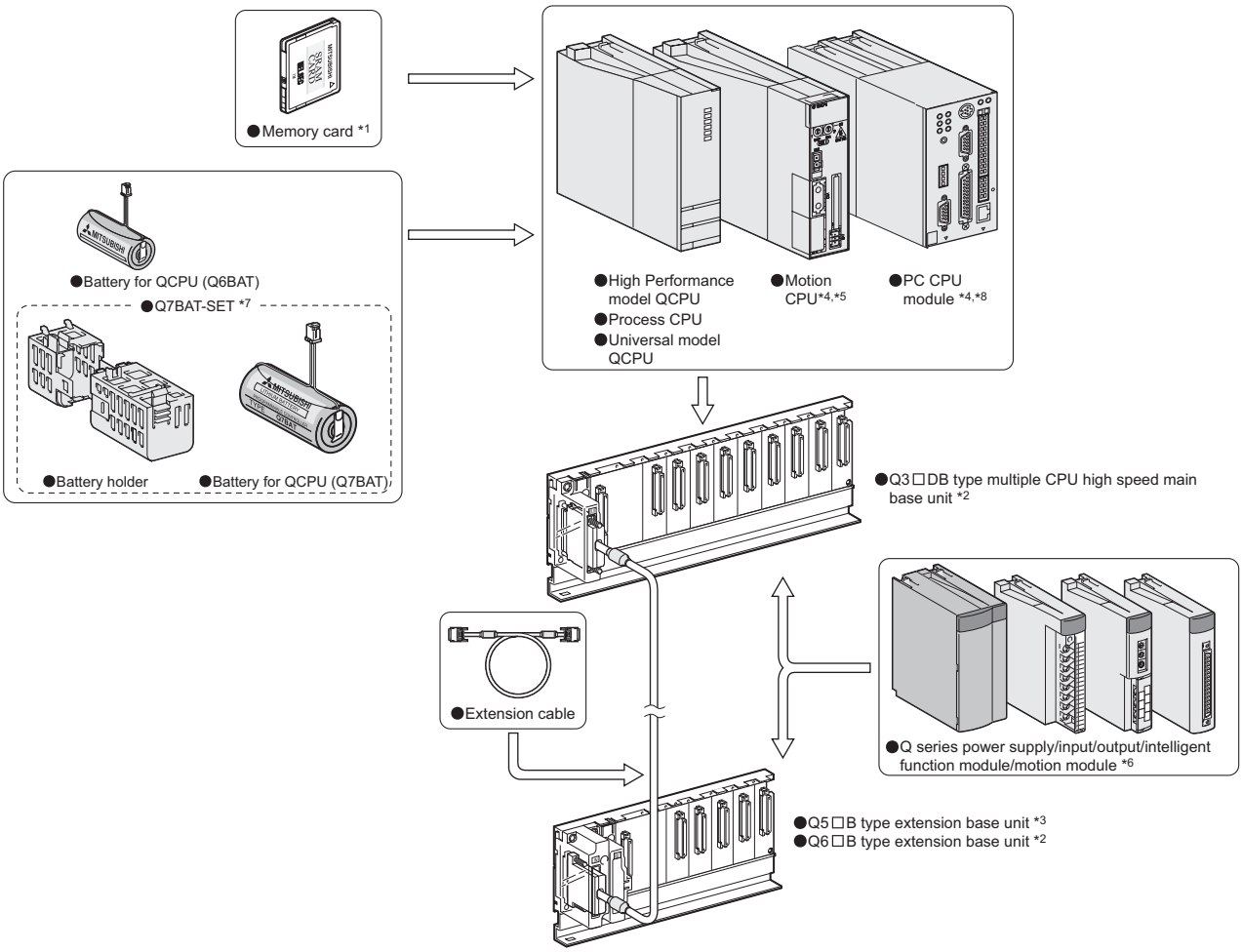
- Do not use an extension cable longer than 13.2m (43.31 ft).
- When using an extension cable, keep it away from the main circuit (high voltage
- and large current) line.
- Set the number of extension stages so as not to be duplicated.
- Although there is no restriction on the connection order of the Q5□B and the Q6□B, check the availability of them by referring to QCPU User's Manual (Hardware Design, Maintenance and Inspection) when both the Q5□B and the Q6□B exist as the extension base unit.
- The QA1S6□B, QA6□B, QA6ADP+A5□B/A6□B, or Q6R□B cannot be connected as an extension base unit.
- Connect the OUT connector of an extension base unit and the IN connector of the adjacent extension base unit by an extension cable.
- When 66 modules or more are mounted, an error "SP. UNIT LAY ERR." (error code: 2124) occurs. (The number of mountable modules includes one CPU module.)
- "No. of CPUs" is the number of CPUs set by [No. of PLC] of GX Developer.
- When mounting the Universal model QCPU and the PC CPU module at the same time, use the PPC-CPU852 (MS)-512 as the PC CPU module.
- The PC CPU module occupies two slots. Therefore, when the PC CPU module is used, the maximum number of I/O modules is decreased by 1 from the value indicated in the table.
- For details of the PC CPU module, refer to the manual of PC CPU module.

2.1.3 System configuration using Universal model QCPU as CPU No.1

The following explains the system configuration using the Universal model QCPU as the CPU No.1.

(1) When using the Multiple CPU High speed main base unit (Q3□DB)

(a) System configuration



* 1: Only one memory card can be mounted. Select an appropriate memory card from the SRAM, Flash and ATA in accordance with application and capacity.
When a commercial memory card is used, the operation is not guaranteed.
* 2: Use the Q series power supply module for the power supply module. Keep the current consumption within the rated output current of the power supply module. The Slim power supply module and Redundant power supply module are not available for the power supply module.
* 3: The Q Series power supply module is not required for the Q5□B extension base unit.
* 4: The motion CPU and PC CPU module do not accept battery for QCPU and memory card.
* 5: Usable Motion CPUs are only the Q172DCPU and Q173DCPUN when the Q03UDCPU, Q04UDHCPU or Q06UDHCPU is used.
Any Motion CPU cannot be mounted with the Q02UCPU.
* 6: Be sure to set the control CPU of the motion module to the Motion CPU.
* 7: When the Q8BAT is used for the Universal model QCPU, use the connection cable whose connector part displays "A".
For details of connector part of a connection cable, refer to the following manual.
☞ QCPU User's Manual (Hardware Design, Maintenance and Inspection)
* 8: For further information on PC CPU module, consult CONTEC Co., Ltd Tel: +81-6-6472-7130)

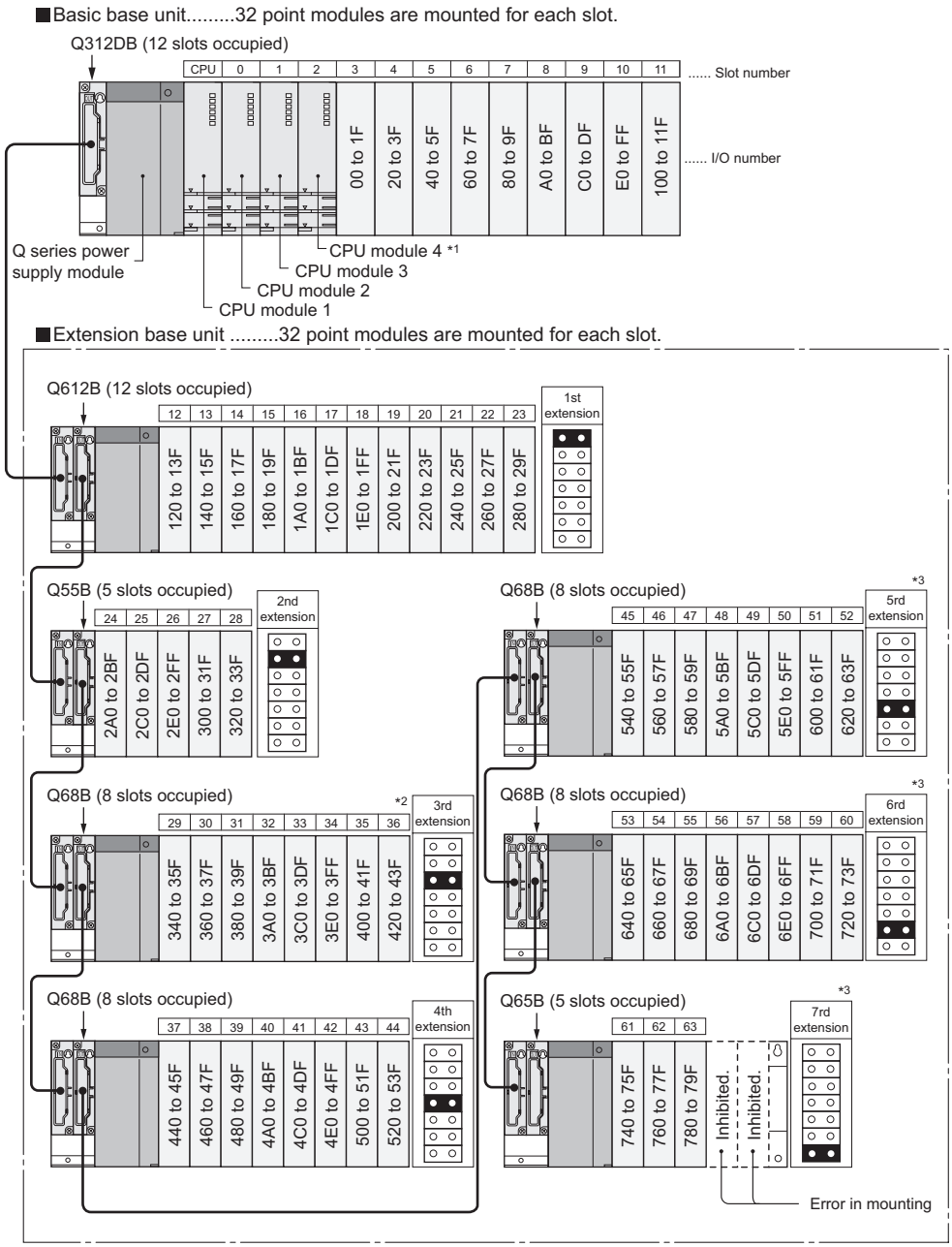
Diagram 2.13 System configuration when Q3□DB is used

POINT

(1) When the multiple CPU system is configured using Q02UCPU as the CPU No.1, only the following CPU modules can be used as the CPUs No.2.
- PC CPU module(PPC-CPU852(MS)-512)

(2) When the multiple CPU system is configured using the Q03UDCPU, Q04UDHCPU, or Q06UDHCPU as the CPU No.1, only the following CPU modules can be used as the CPUs No.2 to No.4.
- Universal model QCPU(except Q02UCPU)
- High Performance model QCPU
- Process CPU
- Motion CPU(Q172DCPU,Q173DCPU)
- PC CPU module(PPC-CPU852(MS)-512)

(b) Outline of system configuration



* 1: When the Q02UCPU is used as the CPU module 1, up to three CPU modulescan be mounted. Therefore, the CPU module 4 does not exist.

* 2: When the Q02UCPU is used as the CPU module 1, the number of mountable modules is 36. Therefore, the module cannot be mounted on slot 36 or later. An error occurs when the module is mounted on slot 36 or later.

* 3: When the Q02UCPU is used as the CPU module 1, up to four extensions can be connected. Therefore, five to seven extensions do not exist.

Diagram 2.14 System configuration example for using Q3□DB

Table2.7 Restrictions on System Configuration, Applicable Base Units, Extension Cables, Power Supply Modules

CPU number	CPU module1: CPU No.1, CPU module 2: CPU No.2, CPU module 3: CPU No.3, CPU module 4: CPU No.4*1	
Maximum number of extension stages	7 extension stages(when the Q02UCPU is used: 4 extension stages)	
Maximum number of mountble I/O modules	65 - (No. of CPUs)(when the Q02UCPU is used: 37-(No. of CPUs))	
Available main base unit model	Q38DB, Q312DB	
Available extension base unit model	Type not requiring power supply module	Q52B, Q55B
	Type requiring Q series power supply module	Q63B, Q65B, Q68B, Q612B
Available extension cable type	QC05B, QC06B, QC12B, QC30B, QC50B, QC100B	
Available power supply module model	Q61P-A1, Q61P-A2, Q61P, Q62P, Q63P, Q64P	

* 1: When the Q02UCPU is mounted on the CPU slot 1, up to three CPU modules can be mounted. Therefore, the CPU module 4 does not exist.

Precautions

- Do not use an extension cable longer than 13.2 m (43.31 ft).
- When using an extension cable, keep it away from the main circuit (high voltage
- and large current) line.
- Set the number of extension stages so as not to be duplicated.
- Although there is no restriction on the connection order of the Q5□B and the Q6□B, check the availability of them by referring to QCPU User's Manual (Hardware Design, Maintenance and Inspection) when both the Q5□B and the Q6□B exist as the extension base unit.
- The QA1S6□B, QA6□B, QA6ADP+A5□B/A6□B, or Q6□RB cannot be used as the extension base unit.
- Connect the OUT connector of an extension base unit and the IN connector of the adjacent extension base unit by an extension cable.
- When 66 modules or more are mounted, an error "SP. UNIT LAY ERR." (error code: 2124) occurs. (The number of mountable modules includes one CPU module.)
- "No. of CPUs" is the number of CPUs set by [No. of PLC] of GX Developer.
- The PC CPU module occupies two slots. Therefore, when the PC CPU module is used, the maximum number of I/O modules is decreased by 1 from the value indicated in the table.
- For details of the Motion CPU,and the PC CPU module, refer to the manual of each CPU module.

(2) When using the main base unit (Q3□B)

(a) System configuration

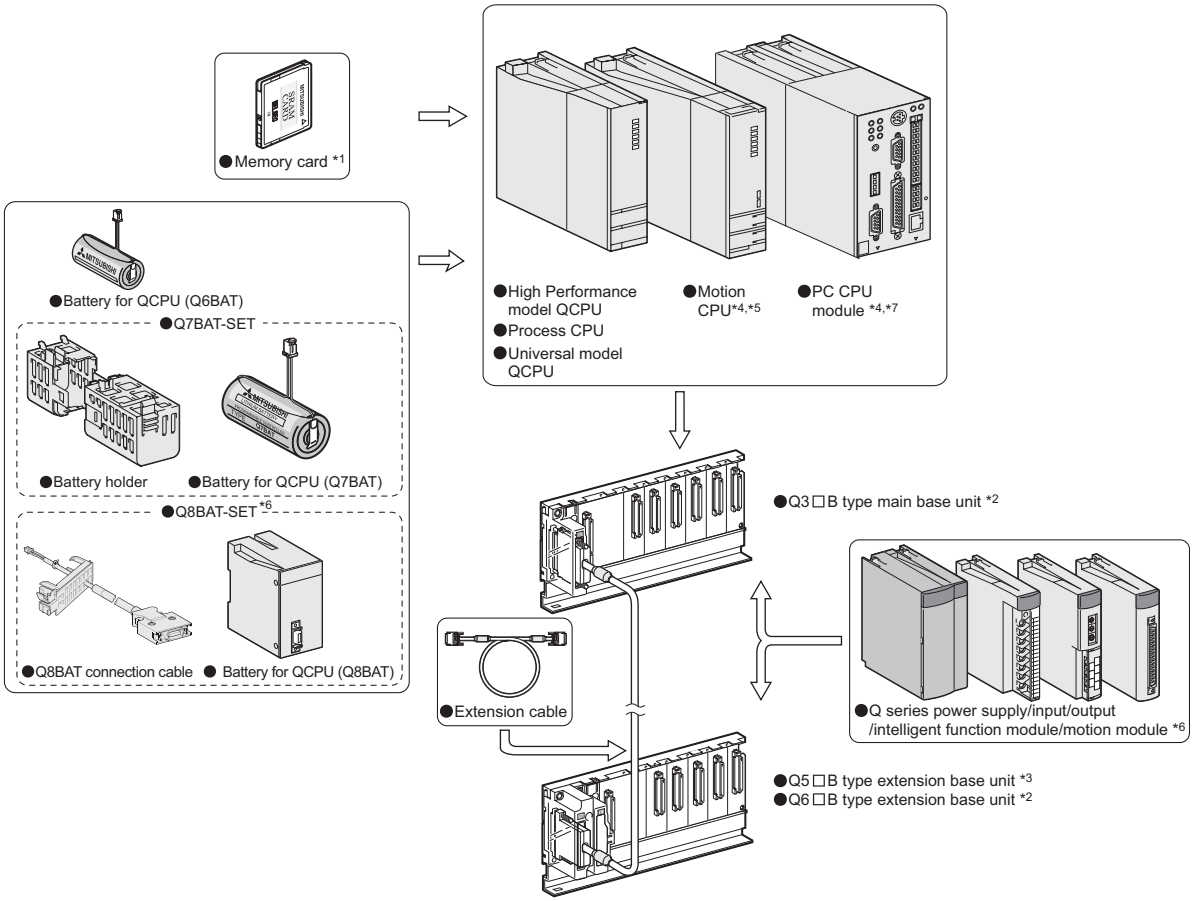


Diagram 2.15 System configuration when Q3□B is used

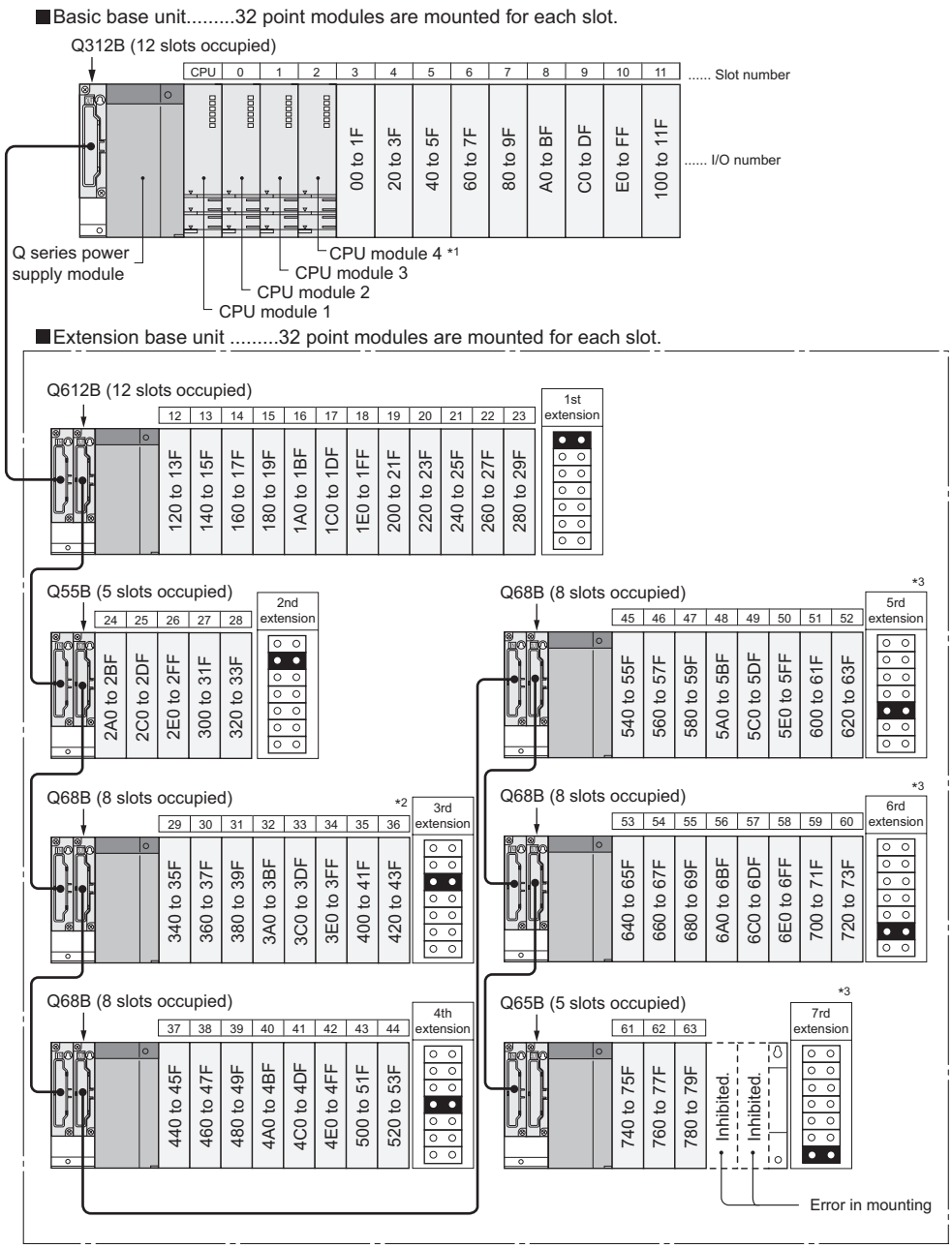
* 1: Only one memory card can be mounted. Select an appropriate memory card from the SRAM, Flash and ATA in accordance with application and capacity.
  When a commercial memory card is used, the operation is not guaranteed.
* 2: Use the Q series power supply module for the power supply module. Keep the current consumption within the rated output current of the power supply module. The Slim power supply module and Redundant power supply module are not available for the power supply module.
* 3: The Q Series power supply module is not required for the Q5□B extension base unit.
* 4: The motion CPU, and PC CPU module do not accept battery for QCPU and memory card.
* 5: Usable Motion CPUs are only the Q172CPUN, Q173CPUN, Q172HCPU, and Q173HCPU when the Q02UCPU is used.
  Any Motion CPU cannot be mounted with the Q03UDCPU, Q04UDHCPU or Q06UDHCPU.
* 6: Be sure to set the control CPU of the motion module to the Motion CPU.
* 7: For further information on PC CPU module, consult CONTEC Co., Ltd Tel: +81-6-6472-7130
* 8: When the Q8BAT is used for the Universal model QCPU, use the connection cable whose connector part displays "A".
  For details of connector part of a connection cable, refer to the following manual.
  ☞ QCPU User's Manual (Hardware Design, Maintenance and Inspection)

POINT

(1) When the multiple CPU system is configured using Q02UCPU as the CPU No.1, only the following CPU modules can be used as the CPUs No.2.
- Motion CPU (Q172CPUN, Q173CPUN, Q172HCPU, and Q173HCPU)
- PC CPU module (PPC-CPU852(MS)-512)

(2) When the multiple CPU system is configured using Q03UDCPU, Q04UDHCPU, Q06UDHCPU as the CPU No.1, only the following CPU modules can be used as the CPUs No.2 to No.4.
- High Performance model QCPU
- Process CPU
- Universal model QCPU (except Q02UCPU)
- PC CPU module (PPC-CPU852(MS)-512)

(b) Outline of system configuration



* 1: When the Q02UCPU is used as the CPU module 1, up to three CPU modulescan be mounted. Therefore, the CPU module 4 does not exist.
* 2: When the Q02UCPU is used as the CPU module 1, the number of mountable modules is 36. Therefore, the module cannot be mounted on slot 36 or later. An error occurs when the module is mounted on slot 36 or later.
* 3: When the Q02UCPU is used as the CPU module 1, up to four extensions can be connected. Therefore, five to seven extensions do not exist.

Diagram 2.16 System configuration example for using Q3□B

Table2.8 Restrictions on System Configuration, Applicable Base Units, Extension Cables, Power Supply Modules

CPU number	CPU module1: CPU No.1, CPU module 2: CPU No.2, CPU module 3: CPU No.3, CPU module 4: CPU No.4*1	
Maximum number of extension stages	7 extension stages (when the Q02UCPU is used: 4 extension stages)	
Maximum number of mountble I/O modules	65 - (No. of CPUs) (when the Q02UCPU is used: 37-(No. of CPUs))	
Available main base unit model	Q33B, Q35B, Q38B, Q312B	
Available extension base unit model	Type not requiring power supply module	Q52B, Q55B
	Type requiring Q series power supply module	Q63B, Q65B, Q68B, Q612B
Available extension cable type	QC05B, QC06B, QC12B, QC30B, QC50B, QC100B	
Available power supply module model	Q61P-A1, Q61P-A2, Q61P, Q62P, Q63P, Q64P	

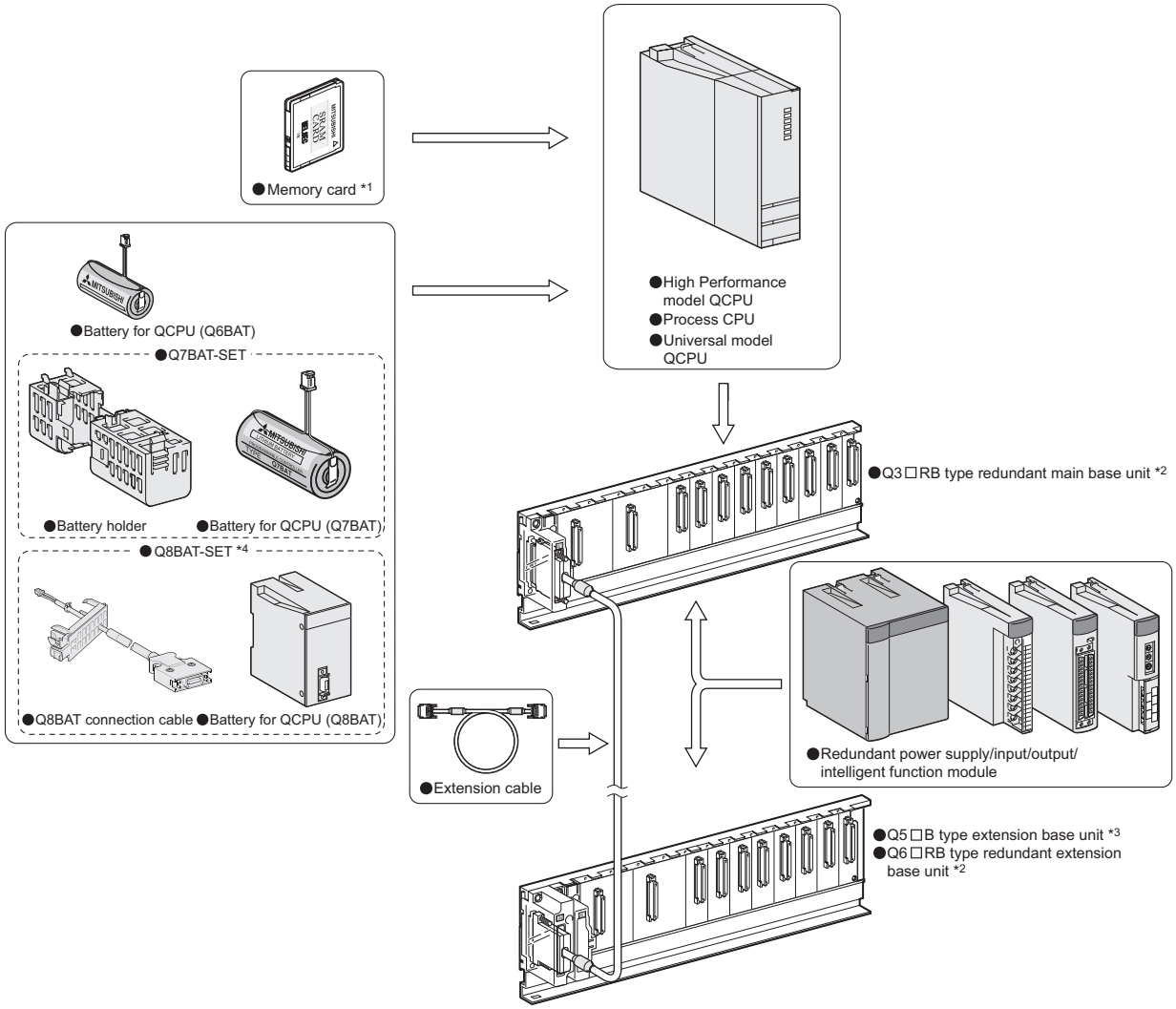
* 1: When the Q02UCPU is mounted on the CPU slot 1, up to three CPU modules can be mounted. Therefore, the CPU module 4 does not exist.

Precautions

- Do not use an extension cable longer than 13.2m (43.31 ft).
- When using an extension cable, keep it away from the main circuit (high voltage and large current) line.
- Set the number of extension stages so as not to be duplicated.
- Although there is no restriction on the connection order of the Q5□B and the Q6□RB, check the availability of them by referring to QCPU User's Manual (Hardware Design, Maintenance and Inspection).
- The QA1S6□B, QA6□B, QA6ADP+A5□B/A6□B, or Q6□RB cannot be connected as an extension base unit.
- Connect the OUT connector of an extension base unit and the IN connector of the adjacent extension base unit by an extension cable.
- When 66 modules or more are mounted, an error "SP. UNIT LAY ERR." (error code: 2124) occurs. (The number of mountable modules includes one CPU module.)
- "No. of CPUs" is the number of CPUs set by [No. of PLC] of GX Developer.
- The PC CPU module occupies two slots. Therefore, when the PC CPU module is used, the maximum number of I/O modules is decreased by 1 from the value indicated in the table.
- For details of the Motion CPU, the PC CPU module and refer to the manual of each CPU module.

(3) When using the redundant main base unit (Q3□RB)

(a) System configuration



* 1: Only one memory card can be mounted. Select an appropriate memory card from the SRAM, Flash and ATA in accordance with application and capacity.
When a commercial memory card is used, the operation is not guaranteed.
* 2: Use the redundant power supply module for the power supply module.
The redundant power supply modules Q63RP and Q64RP can be used on one redundant power supply base unit at the same time.
The Q series power supply module and the slim type power supply module are not available for the power supply module.
* 3: The Q Series power supply module is not required for the Q5□B extension base unit.
* 4: When the Q8BAT is used for the Universal model QCPU, use the connection cable whose connector part displays "A".
For details of connector part of a connection cable, refer to the following manual.
☞ QCPU User's Manual (Hardware Design, Maintenance and Inspection)

Diagram 2.17 System configuration when Q□RB is used

POINT

(1) The Q02UCPU is not available for the multiple CPU system.

(2) When the multiple CPU system is configured using the Universal model QCPU (except Q02UCPU) or the Process CPU as the CPU No.1, only the following modules can be used as the CPUs No.2 to CPU No.4.
- High Performance model QCPU
- Process CPU
- Universal model QCPU (except Q02UCPU)

(3) When duplicating power supply, use the redundant power supply base unit and the redundant power supply module.
For the power supply module mounted on the redundant power supply base unit, only the redundant power supply module can be used.

(b) Outline of system configuration

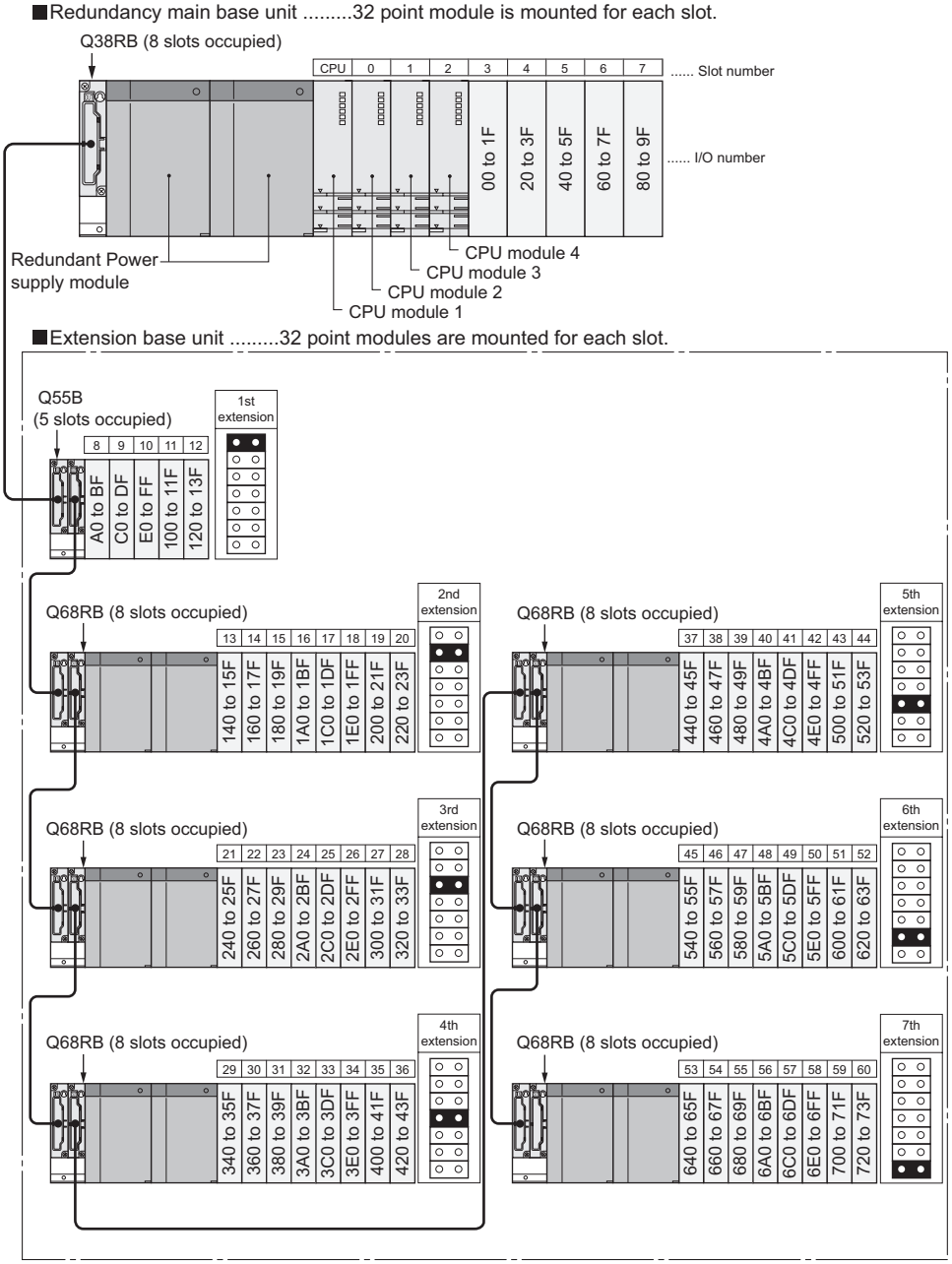


Diagram 2.18 System configuration example for using Q3□RB

Table2.9 Restrictions on System Configuration, Applicable Base Units, Extension Cables, Power Supply Modules

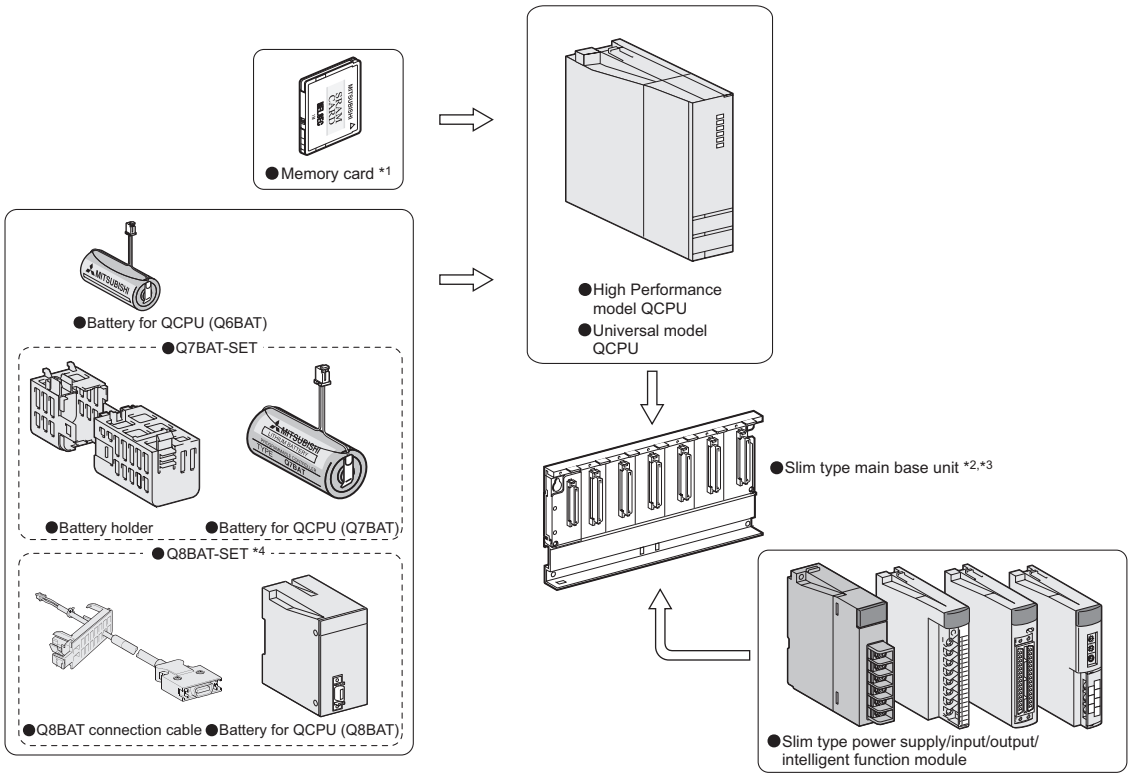
CPU number	CPU module1: CPU No.1, CPU module 2: CPU No.2, CPU module 3: CPU No.3, CPU module 4: CPU No.4	
Maximum number of extension stages	7 extension stages	
Maximum number of mounted I/O modules	65 - (No. of CPUs)	
Available main base unit model	Q38RB	
Available extension base unit model	Type not requiring power supply module	Q52B, Q55B
	Type requiring redundant power supply module	Q68RB
Available extension cable type	QC05B, QC06B, QC12B, QC30B, QC50B, QC100B	
Available power supply module model	Q63RP, Q64RP	

Precautions

- Do not use an extension cable longer than 13.2m (43.31 ft).
- When using an extension cable, keep it away from the main circuit (high voltage and large current) line.
- Set the number of extension stages so as not to be duplicated.
- Although there is no restriction on the connection order of the Q5□B and the Q6R□B, check the availability of them by referring to QCPU User's Manual (Hardware Design, Maintenance and Inspection).
- The Q6□B, QA1S6□B, QA6□B, or QA6ADP+A5□B/A6□B cannot be connected as an extension base unit.
- Connect the OUT connector of an extension base unit and the IN connector of the adjacent extension base unit by an extension cable.
- When 66 modules or more are mounted, an error "SP. UNIT LAY ERR." (error code: 2124) occurs. (The number of mountable modules includes one CPU module.)
- "No. of CPUs" is the number of CPUs set by [No. of PLC] of GX Developer.
- When the redundant power main base unit is used, bus connection is not available for the GOT.
- When the redundant power main base unit is used, the Motion CPU, and PC CPU module cannot be used.

(4) When using the slim type main base unit (Q3□SB)

(a) System configuration



* 1: One memory card is installed. Select an appropriate memory card from the SRAM, Flash and ATA cards according to the application and capacity.
When the memory card is used, operation is not guaranteed.
* 2: The slim type main base unit does not have an extension cable connector.
The extension base or GOT cannot be connected.
* 3: As a power supply module, use the slim type power supply module.
Keep the current consumption within the rated output current of the power supply module.
The Q series power supply module and the redundant power supply module are not available for the power supply module.
* 4: When the Q8BAT is used for the Universal model QCPU, use the connection cable whose connector part displays "A".
For details of connector part of a connection cable, refer to the following manual.
☞ QCPU User's Manual (Hardware Design, Maintenance and Inspection)

Diagram 2.19 System configuration when Q3□SB is used

POINT

(1) The Q02UCPU is not available for the multiple CPU system.
(2) When the multiple CPU system is configured using the Universal model QCPU (except Q02UCPU) as the CPU No.1, only the following CPU modules can be used as the CPUs No.2 and 3.
• High Performance model QCPU
• Universal model QCPU (except Q02UCPU)

(b) Outline of system configuration

■Slim type main base unit .....32 point module is mounted for each slot.

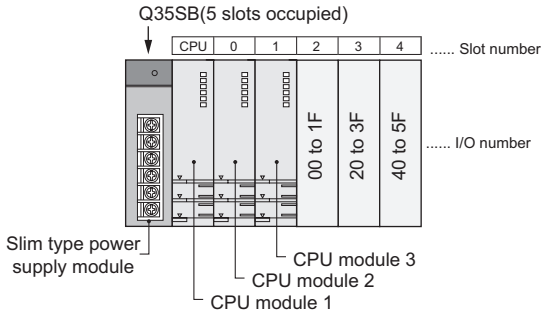


Diagram 2.20 System configuration example for using Q3□SB

Table2.10 Restrictions on System Configuration, Applicable Base Units, Extension Cables, Power Supply Modules

CPU number	CPU module 1: CPU No.1, CPU module 2: CPU No.2, CPU module 3: CPU No.3	
Maximum number of extension stages	Extension not allowed	
Maximum number of mountble I/O modules	Q32SB	3 - (No. of CPUs)
	Q33SB	4 - (No. of CPUs)
	Q35SB	6 - (No. of CPUs)
Available main base unit model	Q32SB, Q33SB, Q35SB	
Available power supply module model	Q61SP	

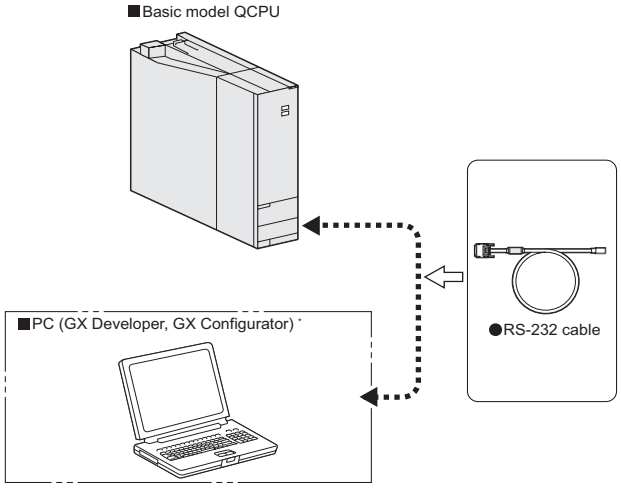
Precautions

- The slim type main base unit has no extension cable connector. The extension base or GOT cannot be connected.
- Since the current consumption of the CPU module exceeds the rated output current of the power supply module (Q61SP), mounting 4 CPU modules is not allowed.
- "No. of CPUs" indicates the number of CPU modules set in the "No. of PLCs" of the GX Developer.

2.2 Configuration of peripheral devices

This section describes the system configurations of peripheral devices that can be used with the Basic model QCPU, High Performance model QCPU, Process CPU and Universal model QCPU.

(1) When using the Basic model QCPU



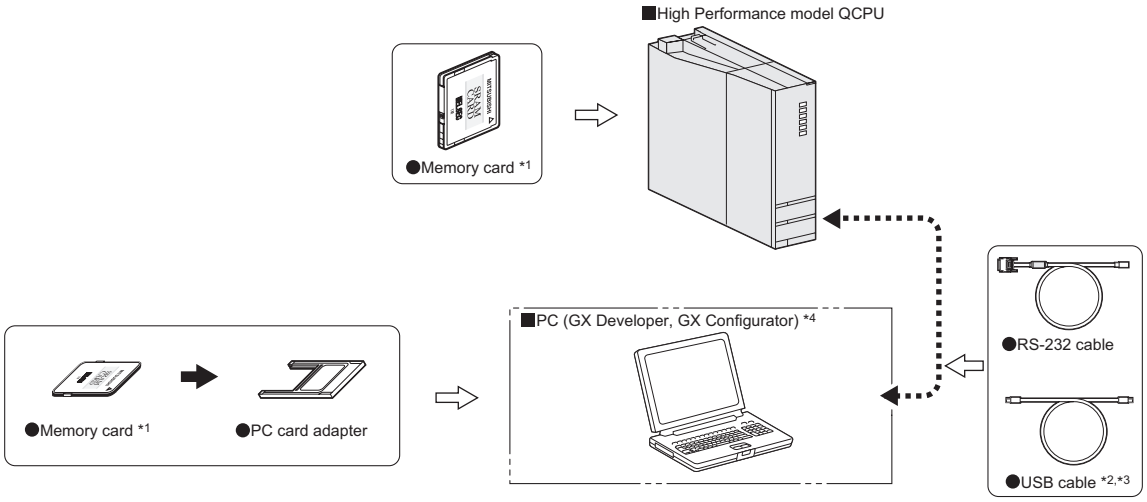
* : The available version varies depending on the system configuration. (☞ Section 2.3)

Diagram 2.21 Configuration of peripheral devices

POINT

For connection between the Motion CPU or PC CPU module and peripheral devices in the multiple CPU system, refer to the relevant manual of each CPU module.

(2) When using the High Performance model QCPU



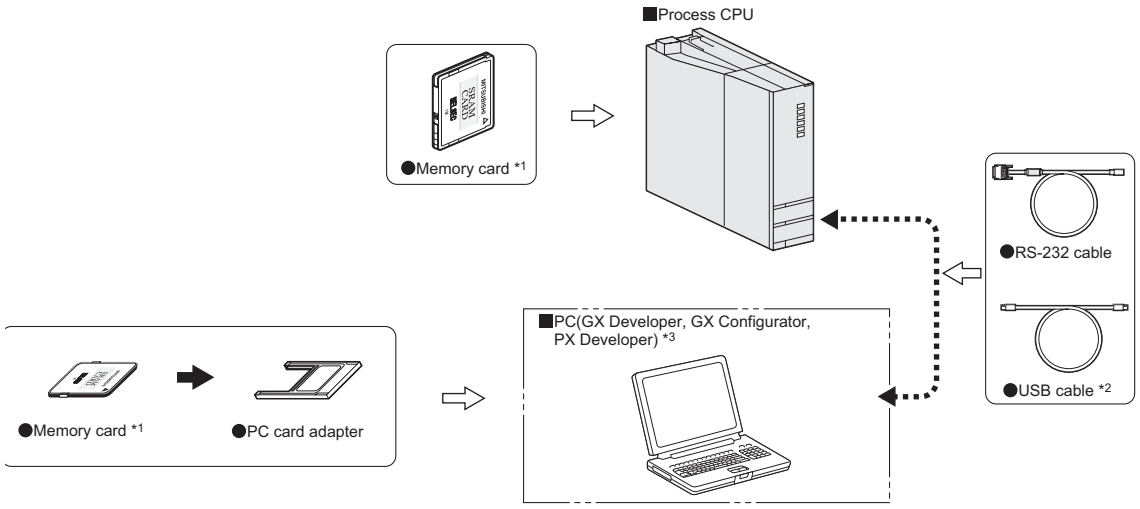
* 1: Do not format the ATA card by other than GX Developer.
  (☞ QCPU User's Manual (Hardware Design, Maintenance and Inspection))
* 2: It is not used for the Q02CPU.
* 3: For writing into memory card by GX Developer and information on USB cables, refer to the operating manual of the GX Developer.
* 4: The available version varies depending on the system configuration. (☞ Section 2.3)

Diagram 2.22 Configuration of peripheral devices

POINT

For connection between the Motion CPU or PC CPU module and peripheral devices in the multiple CPU system, refer to the relevant manual of each CPU module.

(3) When using the Process CPU



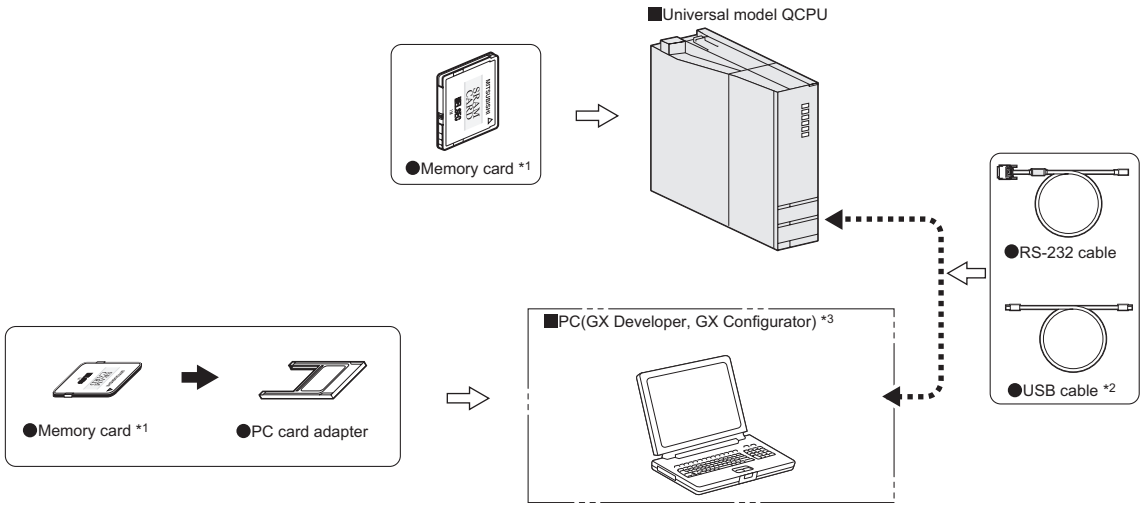
* 1: Do not format the ATA card by other than GX Developer.
  ☞ QCPU User's Manual (Hardware Design, Maintenance and Inspection)
* 2: For writing into memory card by GX Developer and information on USB cables, refer to the operating manual of the GX Developer.
* 3: The available version varies depending on the system configuration. (☞ Section 2.3)

Diagram 2.23 Configuration of peripheral devices

POINT

For connection between the Motion CPU or PC CPU module and peripheral devices in the multiple CPU system, refer to the relevant manual of each CPU module.

(4) When using the Universal model QCPU



* 1: Do not format the ATA card by other than GX Developer.
  ☞ QCPU User's Manual (Hardware Design, Maintenance and Inspection)
* 2: For writing into memory card by GX Developer and information on USB cables, refer to the operating manual of the GX Developer.
* 3: The available version varies depending on the system configuration. (☞ Section 2.3)

Diagram 2.24 Configuration of peripheral devices

POINT

For connection between the Motion CPU or PC CPU module and peripheral devices at the configuration of the Multiple CPU system, refer to the relevant manual of each CPU module.

2.3 Configurable device and available software

Information on devices and software packages used for the system configuration is described in this section.

(1) CPU modules available for multiple CPU system

There are some restrictions on the CPU module model and function version as shown in the table below.

The restriction of each CPU module is explained in Table2.11 to Table2.13.

(a) When Basic model QCPU is used

Table2.11 Available CPU modules

CPU module	Model	Restrictions
Basic model QCPU *1	Q00CPU,Q01CPU	Function version B or later
Motion CPU *2	Q172CPUN,Q173CPUN, Q172HCPU,Q173HCPU	Refer to each CPU manual
PC CPU module	PPC-CPU686(MS)-64, PPC-CPU686(MS)-128 PPC-CPU852(MS)-512	

* 1: The Q00JCPU is not available for the multiple CPU system.
* 2: When using the Motion CPU, install OS software.
For the OS types and versions, refer to the Motion CPU manual.

(b) When High Performance model QCPU or Process CPU is used as CPU No.1

Table2.12 Available CPU modules

CPU module	Model	Restrictions
High Performance model QCPU*2	Q02CPU,Q02HCPU,Q06HCPU, Q12HCPU,Q25HCPU	Function version B or later
Process CPU	Q12PHCPU,Q25PHCPU	No version restriction
Universal model QCPU	Q03UDCPU,Q04UDHCPU, Q06UDHCPU	No version restriction
Motion CPU *1	Q172CPUN,Q173CPUN, Q172HCPU,Q173HCPU	Refer to each CPU manual
PC CPU module *2	PPC-CPU686(MS)-64, PPC-CPU686(MS)-128 PPC-CPU852(MS)-512	

* 1: When using the Motion CPU, install OS software.
For the OS types and versions, refer to the Motion CPU manual.
* 2: When using the High Performance model QCPU together, use the following High Performance model QCPU.
• Function version B with the first 5 digits of the serial number, "03051" or later

(c) When Universal model QCPU is used as CPU No.1

Table2.13 Available CPU modules

CPU module	Model	Restrictions
Universal model QCPU	Q03UDCPU,Q04UDHCPU, Q06UDHCPU	No version restriction
High Performance model QCPU	Q02CPU,Q02HCPU,Q06HCPU, Q12HCPU,Q25HCPU	Function version B or later
Process CPU	Q12PHCPU,Q25PHCPU	No version restriction
Motion CPU	Q172DCPU,Q173DCPU	Refer to each CPU manual
PC CPU module	PPC-CPU852(MS)-512	

(2) Precautions when using Q Series I/O modules and intelligent function modules

(a) Compatible I/O modules

All I/O modules (QX□, QY□) are compatible with the multiple CPU system.
They can be used by setting any of CPU No.1 to No.4 as a control CPU.

(b) Compatible intelligent function modules

1) The intelligent function modules compatible with the multiple CPU system are those of function version B or later.
They can be used by setting any of CPU No.1 to No.4 as a control CPU.

2) Q Series high speed counter modules (QD62, QD62D, QD62E) compatible with the multiple CPU system are those of function version A or later.
They can be used by setting any of CPU No.1 to No.4 as a control CPU.

3) Q Series interrupt modules (QI60) do not have a function version, but are supported by the multiple CPU system.
CPUs No.1 to No.4 can be set up as control CPUs.

4) Intelligent function modules of function version A can be used in the multiple CPU system by setting CPU No.1 as a control CPU.
However, only control CPU can be accessed from serial communication modules and other external modules. (MELSECNET/H, serial communication modules and other external modules cannot access non-control CPUs.)
The "SP. UNIT VER. ERR. (error code: 2150)" occurs if any of CPU No.2 to No.4 has been set as a control CPU, and the multiple CPU system will not start up.

(c) Ranges of access to controlled and non-controlled modules

In a multiple CPU system, non-controlled modules can be accessed by setting "Out-of-group I/O setting" at the "Multiple CPU settings" dialog box in "PLC Parameter".
Refer to Section 3.4 for the details about accessibility to the controlled and non-controlled modules in the multiple CPU system.

(3) Module replaceable online

(a) I/O modules and intelligent function modules

When a multiple CPU system includes a Process CPU, online module change is allowed.

The modules controlled by the Process CPU can be changed online.

The modules controlled by the High Performance model QCPU, Motion CPU, PC CPU module and Universal model QCPU cannot be changed online.

Modules changeable online are shown in Table2.14.

Table2.14 Modules replaceable online

Module type		Restriction
Input module		No restriction
Output module		
I/O composite module		
Intelligent function module	Analog-digital converter module	Function version "C" or later
	Digital-analog converter module	
	Thermocouple input module	
	Temperature control module	
	Pulse input module	

(b) CPU modules

To replace a module used with the Process CPU without stopping the system, configure a multiple CPU system with the CPU modules given in Table2.15.

Table2.15 CPU modules supporting online module change

CPU Module Type	Model	Function Version/Serial No.
High Performance model QCPU	Q02CPU,Q02HCPU,Q06HCPU, Q12HCPU,Q25HCPU	First 5 digits of serial No. "04012" or later
Process CPU	Q12PHCPU,Q25PHCPU	No version restriction
Universal model QCPU	Q03UDCPU,Q04UDHCPU, Q06UDHCPU	
Motion CPU	Q172CPUN,Q173CPUN	Version "A" or later
	Q172HCPU,Q173HCPU	
PC CPU module	PPC-CPU686(MS)-64, PPC-CPU686(MS)-128, PPC-CPU852(MS)-512	Bus interface driver (PPC-DRV-01) version "1.05" or later

(4) Applicable software

(a) GX Developer and PX Developer

Versions of the GX Developer and the PX Developer applicable in the multiple CPU system are shown in Table2.16.

Table2.16 Applicable GX Developer and PX Developer

QCPU	Applicable software version	
	GX Developer	PX Developer
Basic model QCPU *2	Version 8.00A or later	Use not allowed
High Performance model QCPU	Version 6.00A or later	
Process CPU	Version 7.10L or later *1	Version 1.00A or later
Universal model QCPU	Version 8.48A or later	Use not allowed

* 1: When using PX Developer, use GX Developer of version 7.12N or later.
* 2: The Q00JCPU is not available for the multiple CPU system.

(b) Applicable GX Configurator

Versions of GX Configurator applicable in the multiple CPU system are shown in Table2.17.

Table2.17 Applicable GX Configurator

QCPU	Applicable software version	
	Product name	Version
Basic model QCPU	GX Configurator-AD	Version 1.10L or later *1, *2
	GX Configurator-DA	Version 1.10L or later *3
	GX Configurator-SC	Version 1.10L or later
	GX Configurator-CT	Version 1.10L or later *4
	GX Configurator-TI	Version 1.10L or later *5, *6
	GX Configurator-TC	Version 1.10L or later
	GX Configurator-FL	Version 1.10L or later
	GX Configurator-QP	Version 2.10L or later
	GX Configurator-PT	Version 1.10L or later
	GX Configurator-AS	Version 1.13P or later
	GX Configurator-MB	Version 1.00A or later
	GX Configurator-DN	Version 1.10L or later
High performance model QCPU	GX Configurator-AD	SW0D5C-QADU 20C or later *1, *2
	GX Configurator-DA	SW0D5C-QDAU 20C or later *3
	GX Configurator-SC	SW0D5C-QSCU 20C or later *7
	GX Configurator-CT	SW0D5C-QCTU 20C or later *4
	GX Configurator-TI	Version 1.00A or later *5, *6
	GX Configurator-TC	SW0D5C-QCTU 00A or later
	GX Configurator-FL	SW0D5C-QFLU 00A or later
	GX Configurator-QP	Version 2.00A or later
	GX Configurator-PT	Version 1.00A or later
	GX Configurator-AS	Version 1.13P or later
	GX Configurator-MB	Version 1.00A or later
	GX Configurator-DN	Version 1.00A or later
Process CPU	GX Configurator-AD	Version 1.13P or later *1, *2
	GX Configurator-DA	Version 1.13P or later *3
	GX Configurator-SC	Version 1.13P or later
	GX Configurator-CT	Version 1.13P or later *4
	GX Configurator-TI	Version 1.13P or later *6
	GX Configurator-TC	Version 1.13P or later
	GX Configurator-FL	Version 1.13P or later
	GX Configurator-QP	Version 2.13P or later
	GX Configurator-PT	Version 1.13P or later
	GX Configurator-AS	Version 1.13P or later
	GX Configurator-MB	Version 1.00A or later
	GX Configurator-DN	Version 1.13P or later

* 1: When using the Q64AD-GH, use version 1.13P or later.
* 2: When using the Q62AD-DGH, use version 1.14Q or later.
* 3: When using the Q62DA-FG, use version 1.14Q or later.
* 4: When using the QD60P8-G, use version 1.14Q or later.
* 5: When using the Q64TDV-GH, use version 1.13P or later.
* 6: When using the Q64RD-G, use version 1.17T or later.
* 7: When using the QJ71CMO, use version 1.10L or later.

Table2.17 Applicable GX Configurator (continued)

QCPU	Applicable software version	
	Product name	Version
Universal model QCPU	GX Configurator-AD	Version 2.05F or later
	GX Configurator-DA	Version 2.06G or later
	GX Configurator-SC	Version 2.12N or later
	GX Configurator-CT	Version 1.25B or later
	GX Configurator-TI	Version 1.24A or later
	GX Configurator-TC	Version 1.23Z or later
	GX Configurator-FL	Version 1.23Z or later
	GX Configurator-QP	Version 2.24A or later
	GX Configurator-PT	Version 1.23Z or later
	GX Configurator-AS	Version 1.22Y or later
	GX Configurator-MB	Version 1.08J or later
	GX Configurator-DN	Version 1.23Z or later

2.4 Precautions for system configuration

Restrictions on the system configuration using the Q series CPU module are provided in this section.

(1) Modules of restricted quantity

The number of mountable modules and supported functions are restricted depending on the module type.
For the number of modules that can be mounted for each Motion CPU or PC CPU module, refer to each CPU module manual.

(a) When using the Basic model QCPU

Table2.18 Modules of restricted quantity

Product	Model	Number of modules that can be mounted per system	Quantity restriction per QCPU
Q series MELSECNET/H network module	• QJ71LP21 • QJ71BR11 • QJ71LP21-25 • QJ71LP21S-25 • QJ71LP21G • QJ71LP21GE	Up to 4 modules on the PLC to PLC network. (However, the module that can be controlled by the Basic model QCPU is only one module on the PLC to PLC network)	One module only on the PLC to PLC network
Q series Ethernet interface module	• QJ71E71 • QJ71E71-B2 • QJ71E71-B5 • QJ71E71-100	Only 1 module (Controllable with QCPU only)	Only 1 module
Q series CC-Link system master/ local module	• QJ61BT11 • QJ61BT11N	Up to 10 modules *1 (Up to 2 modules can be controlled by QCPU.)	Up to 2 modules *1
Interrupt module	• QI60	Up to 3 modules *2 (Only 1 module can be controlled by QCPU.)	Only 1 module *2
GOT	• GOT-A900 series (Bus connection only) *3 • GOT1000 series (Bus connection only) *3	Up to 5 modules	Up to 5 modules

* 1: Modules of function version B or later can be used.
* 2: Indicates the number of interrupt modules to which the interrupt pointer setting has not been made.
When the interrupt pointer setting has been made, the number of modules are not restricted.
* 3: For the available GOT model name, refer to the following manuals.
☞ GOT-A900 Series User's Manual (GT Works2 Version2/GT Designer2 Version2 compatible Connection System Manual)
☞ GOT1000 Series Connection User's Manual

(b) When using the High Performance model QCPU, Process CPU

Table2.19 Modules of restricted quantity

Product	Model	Number of modules that can be mounted per system		Quantity restriction per QCPU	
Q series MELSECNET/G network module *5	• QJ71GP21-SX • QJ71GP21S-SX	Up to 2 modules	Up to 4 modules	Up to 2 modules	Up to 4 modules
Q series MELSECNET/H network module	• QJ71LP21 • QJ71BR11 • QJ71LP21-25 • QJ71LP21S-25 • QJ71LP21G • QJ71LP21GE	Up to 4 modules		Up to 4 modules	
Q series Ethernet interface module	• QJ71E71 • QJ71E71-B2 • QJ71E71-B5 • QJ71E71-100	Up to 4 modules		Up to 4 modules	
Q series CC-Link system master/ local module	• QJ61BT11 • QJ61BT11N	No restriction *1		No restriction *1	
AnS series corresponding special function module *2	• A1SJ71PT32-S3 • A1SJ71T32-S3	No restriction (Auto refresh setting not allowed)		No restriction (Auto refresh setting not allowed)	
	• A1SD51S • A1SD21-S1 • A1SJ71J92-S3 • (When using GET/PUT service)	Up to 6 modules		Up to 6 modules	
Interruption module	• A1SI61 *2	Only 1 module		Only 1 module*4	
	• QI60	Up to 4 modules*4 (Up to 3 modules when the A1SI61 is in use)			
GOT	• GOT-A900 series (Bus connection only) *3 • GOT1000 series (Bus connection only) *3	Up to 5 modules		Up to 5 modules	

* 1: One CPU module with CC-Link network parameter setting in GX Developer can control the following number of the CC-Link master/local modules.
  • The CPU module whose first five digits of a serial number is 08031 or lower: up to 4
  • The CPU module whose first five digits of a serial number is 08032 or higher: up to 8
* 2: This module can be used when a High Performance model QCPU is set to a controlled module. When the Process CPU is used in conbimation, however, it cannot be used. (☞ Section 7.1)
* 3: For the available GOT model name, refer to the following manuals.
  When the Universal model QCPU is used, GOT-A900 Series cannot be used.
  ☞ GOT-A900 Series User's Manual (GT Works2 Version2/GT Designer2 Version2 compatible Connection System Manual)
  ☞ GOT1000 Series Connection User's Manual
* 4: Only the High Performance model QCPU whose first 5 digits of serial No. is 09012 or later is applicable.

POINT

For restrictions on mounting the A series module on the QA6□B, QA6ADP+A5□B/A6□B refer to the following manual.
☞ QA65B/QA68B Extension Base Unit User's Manual
☞ QA6ADP QA Conversion Adapter Module

(c) When using the Universal model QCPU

Table2.20 Modules of restricted quantity

Product	Model	Number of modules that can be mounted per system	Quantity restriction per QCPU
Q series MELSECNET/G network module	• QJ71GP21-SX • QJ71GP21S-SX	Up to 4 modules *4	Up to 4 modules *4
Q series MELSECNET/H network module	• QJ71LP21 • QJ71BR11 • QJ71LP21-25 • QJ71LP21S-25 • QJ71LP21G • QJ71LP21GE		
Q series Ethernet interface module	• QJ71E71 • QJ71E71-B2 • QJ71E71-B5 • QJ71E71-100	Up to 4 modules *4	Up to 4 modules *4
Q series CC-Link system master/ local module	• QJ61BT11N	No restriction *1	No restriction *1
Interruption module	• QI60	Up to 4 modules *3	Only 1 module *3
GOT	• GOT1000 series (Bus connection only) *2	Up to 5 modules	Up to 5 modules

* 1: One CPU module with CC-Link network parameter setting in GX Developer can control the following number of the CC-Link master/local modules.
  • Q02UCPU: up to 4
  • Q03UDCPU,Q04UDHCPU,Q06UDHCPU: up to 8
  There is no restriction on the number of mountable modules when setting parameters with the CC-Link dedicated instructions.
  ☞ CC-Link Master/Local Module User's Manual
* 2: For the model name of the applicable GOT, refer to the following manual.
  ☞ GOT1000 Series Connection System Manual
* 3: The number of interrupt modules where the interrupt pointer setting is not made is shown. If set, there is no restriction on the number of mountable modules.
* 4: As for the Q02UCPU, both the number of mountable modules per QCPU and the number of mountable modules per system are up to two respectively.

(2) Combination of power supply module, base unit and QCPU

Combination of power supply module, base unit and QCPU has some restrictions. For details, refer to the following:

☞ QCPU User's Manual (Hardware Design, Maintenance and Inspection)

(Example) The redundant power supply module (Q64RP) can be mounted only on the redundant main base unit (Q38RB) or the redundant extension base unit (Q68RB).

(3) Precautions for using QCPU of function version A

When the multiple CPU system has been configured using a QCPU of function version A, an error occurs and the multiple CPU system is not started.
Errors shown in Table2.21 will occur and the multiple CPU system will not start up if function version A High Performance model QCPUs and High Performance model QCPU/Process CPU are used on a multiple CPU system.
If any of the errors shown in Table2.21 are displayed after executing the CPU diagnosis function of GX Developer Version 6 or later, replace the High Performance model QCPU of function version A with that of a function version B.

Table2.21 List of operations for each case

CPU No.1	CPU Nos. 2 to 4	Status of CPU No.1	Status of CPU Nos. 2 to 4
High Performance model QCPU of function version A	High Performance model QCPU of function version A	UNIT VERIFY ERR. (error code:2000)	SP.UNIT LAY ERR. (error code:2125)
High Performance model QCPU of function version A	High Performance model QCPU/Process CPU of function version B	UNIT VERIFY ERR. (error code:2000)	MULTI EXE.ERROR *1 (error code:7010)
High Performance model QCPU/Process CPU of function version B	High Performance model QCPU of function version A	MULTI EXE.ERROR *1 (error code:7010)	SP.UNIT LAY ERR. (error code:2125)
High Performance model QCPU/Process CPU of function version B	High Performance model QCPU/Process CPU of function version B	No error	No error

* 1: The following errors may occur except "MULTI EXE. ERROR" when the PLC is turned on or the High Performance model QCPU for CPU No.1 is reset.
"CONTROL-BUS ERR. (error code:1413/1414)"
"MULTI CPU DOWN (error code:7000/7002)"

Basic Process Universal
Note2.1

(4) Precautions for use of high speed interrupt function*Note2.1*

Some system configurations and functions are restricted when the "High speed interrupt fixed scan interval" setting has been mad with a parameter.
☞ QCPU User's Manual (Function Explanation, Program Fundamentals)

Note that the above restrictions do not apply to the High Performance model QCPU of serial number "04011" or earlier since it ignores the "High speed interrupt fixed scan interval" setting.

(5) Precautions for use of Motion CPU(Q172DCPU,Q173DCPU)

When the Q172/ Q173DCPUs are used, the main base unit can use the multiple CPU high speed main base unit for Multiple CPU system only.
However, do not mount the motion modules to 0 to 2 of the multiple CPU high speed main base unit for Multiple CPU system.
☞ Manual for Motion CPU

Universal
Note2.2

(6) Precautions for GOT connection*Note2.2*

Only the GOT-A900 and GOT-F900 series (Basic OS compatible with Q mode and communication driver must be installed) and GOT1000 series can be used.
The GOT800 series, A77GOT, and A64GOT cannot be used.

Basic Process Universal
Note2.1

For the Basic model QCPU, the Process CPU and the Universal model QCPU, the high speed interrupt function is not available.

Universal
Note2.2

For the Universal model QCPU, GOT-A900 and GOT-F900 series are not available. Only 1000 series is available.

CHAPTER3 CONCEPT FOR MULTIPLE CPU SYSTEM

3.1 Mounting position of CPU module

For the configuration of the multiple CPU system, the combination of CPU modules shown in Table3.1 is available.

Table3.1 Combination of CPU modules

CPU module No.1		Number of CPU that can be mounted on CPU module No.2 or later					Maximum number of mounted modules (including CPU module No.1)	Reference
		High Performance model QCPU/ Process CPU/ Universal model QCPU	Motion CPU		PC CPU module			
			Q172CPUN Q173CPUN Q172HCPU Q173HCPU	Q172DCPU Q173DCPU	PPC-CPU686(MS)-64 PPC-CPU686(MS)-128	PPC-CPU852(MS)-512		
Basic model QCPU		----	0 to 1	----	0 to 1		3	Section 3.1.1
High Performance model QCPU/Process CPU		0 to 3	0 to 3	----	0 to 1		4	Section 3.1.2
Universal model QCPU	Q02UCPU	----	0 to 1	----	----	0 to 1	3	Section 3.1.3
	Q03UDCPU Q04UDHCPU Q06UDHCPU	0 to 3	----	0 to 3	----	0 to 1	4	

---- : indicates combination is impossible.

3.1.1 When CPU No.1 is Basic model QCPU

The mounting position of each CPU module is shown in Table3.2.

(1) Mounting position of Basic model QCPU

Only one Basic model QCPU can be mounted on the CPU slot (slot on the right-hand side of the power supply module) of the main base unit.

(2) Mounting position of Motion CPU

Only one Motion CPU can be mounted to slot 0 on the right of the Basic model QCPU. It cannot be mounted to other than slot 0.

(3) Mounting position of PC CPU module

Either one of the PC CPU module can be mounted on the right edge of the CPU module.
(No CPU module can be mounted on the right side of the PC CPU module.)

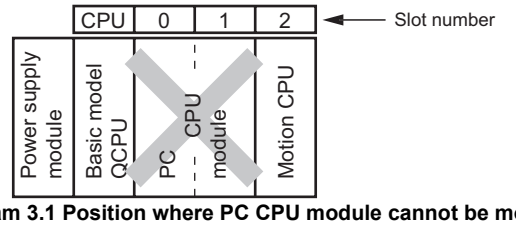


Diagram 3.1 Position where PC CPU module cannot be mounted

(a) When mounting the Motion CPU

• The PC CPU module can be mounted on slot 1 or 2.

(b) When not mounting the Motion CPU

• The PC CPU module can be mounted on slot 0 or 1.

(4) "PLC (Empty)" setting

An empty slot can be reserved for future addition of a CPU module.
Select the number of CPU modules including empty slots on No. of PLC and set the type of the slots to be emptied to "PLC (Empty)" on I/O assignment of PLC parameter.

(a) When adding the Motion CPU in the future.

Set slot 0 as "PLC (Empty)."

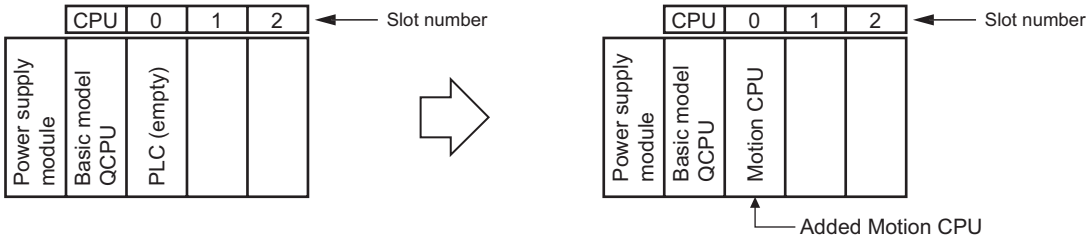


Diagram 3.2 "PLC (Empty)" setting for addition of Motion CPU

(b) When adding the PC CPU module in the future.

1) When mounting the Motion CPU
Set slot 1 as "PLC (Empty)."

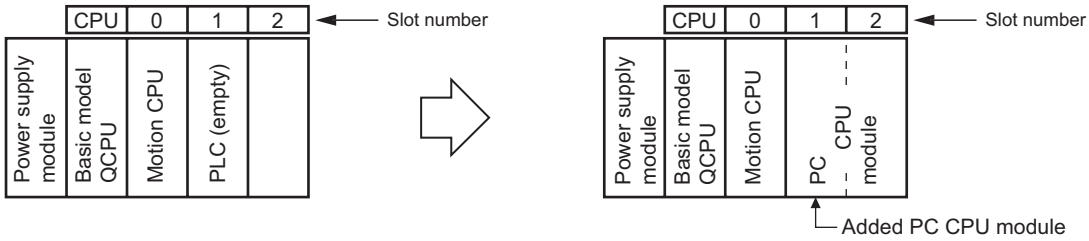


Diagram 3.3 "PLC (Empty)" setting for addition of PC CPU

2) When not mounting CPU
Set slot 0 as "PLC (Empty)."

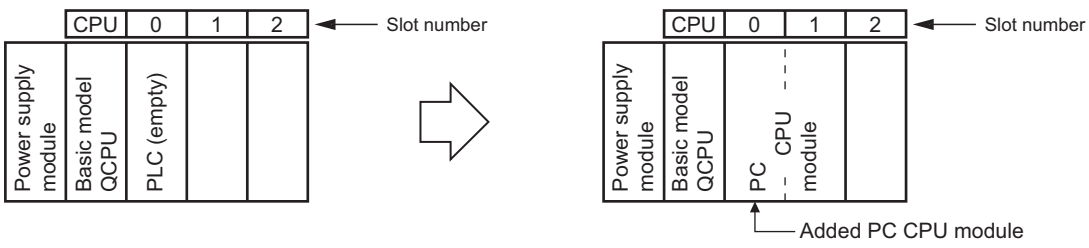


Diagram 3.4 "PLC (Empty)" setting for addition of PC CPU

POINT

Therefore, even when adding the Motion CPU to the system where the Basic model QCPU and the PC CPU in the future, CPU No. of the PC CPU module is not changed. Therefore, the program does not have to be changed.

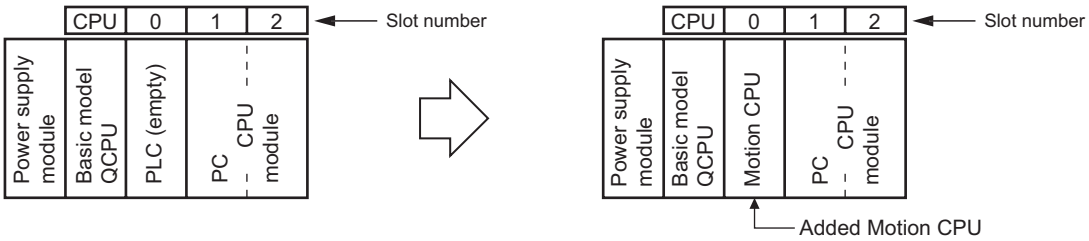


Diagram 3.5 "PLC (Empty)" setting between CPU modules

Table3.2 Mounting position of CPU module

CPU | 0 | 1 | 2 : Slot number

No. of CPUs*1	Mounting position of CPU module		
2	Power supply module / Basic model QCPU / Motion CPU /	Power supply module / Basic model QCPU / PC*2 CPU module /	Power supply module / Basic model QCPU / PLC (empty) / *3
3	Power supply module / Basic model QCPU / Motion CPU / PC*2 CPU module /	Power supply module / Basic model QCPU / Motion CPU / PLC (empty) / *4	Power supply module / Basic model QCPU / CPU (empty) / PC*2 CPU module /
	Power supply module / Basic model QCPU / PLC (empty) / PLC (empty) / *4	----	----

* 1: No. of CPUs indicates the value set in the multiple CPU setting of the PLC parameter.
* 2: The PC CPU module occupies 2 slots.
* 3: When mounting a PC CPU module to slot 0 in the future, do not mount any module to slot 1.
* 4: When mounting a PC CPU module to slot 1 in the future, do not mount any module to slot 2.

3.1.2 When CPU No.1 is High Performance model QCPU or Process CPU

The mounting position of each CPU module is shown in Table3.3.

(1) Mounting position of High Performance model QCPU or Process CPU

Up to four modules of High Performance model QCPUs or Process CPUs can be mounted from the CPU slot (the slot on the right side of power supply module) to slot 2.

There must be no empty slot between CPU modules.

(2) Mounting position of Universal model QCPU

Up to three Universal model QCPU can be mounted on slots 0 to 2 of the main base unit.

(3) Mounting position of Motion CPU

Next to the right side of the High Performance model QCPU, Process CPU, or Universal model QCPU, up to three Motion CPUs can be mounted on slots 0 to 2.

The High Performance model QCPU, Process CPU, or Universal model QCPU cannot be mounted on the right side of the Motion CPU.

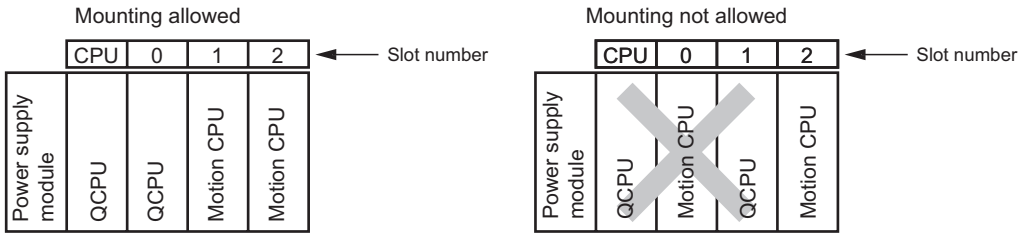


Diagram 3.6 Mounting position of Motion CPU

(4) Mounting position of PC CPU module

Only one PC CPU module can be mounted on the right side of the other CPU modules.

(No CPU module can be mounted on the right side of the PC CPU module.)

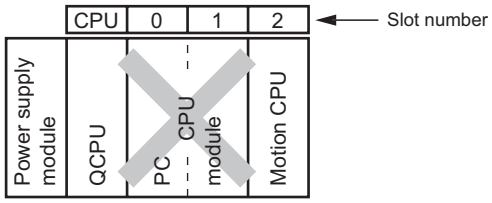


Diagram 3.7 Position where PC CPU module cannot be mounted

(5) "PLC (Empty)" setting

An empty slot can be reserved for future addition of a CPU module.
Set the number of CPU modules including empty slots in the number of CPUs setting, and set the type of the empty slot as "PLC (Empty)" from the right side slot of the mounted CPU module in order with the I/O setting in the PLC Parameter.
(Example)When 4 CPU modules have been set in the multiple CPU setting and 2 High Performance model QCPUs and one Motion CPU are to be mounted.
Mount the High Performance model QCPUs in the CPU slot and slot 0 and the Motion CPU in slot 1, and leave slot 2 "PLC (empty)."

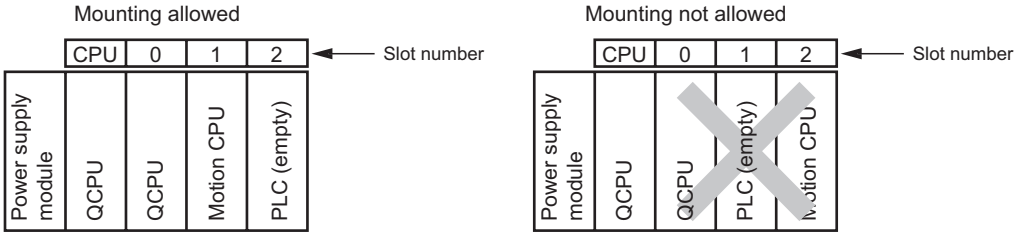


Diagram 3.8 "PLC (Empty)" setting

POINT

When using the High Performance model QCPU or Process CPU, "PLC (Empty)" cannot be set between CPU modules.
To add a CPU module to the system where the PC CPU module is used, move the PC CPU module to the right to make room for the CPU module to be added.

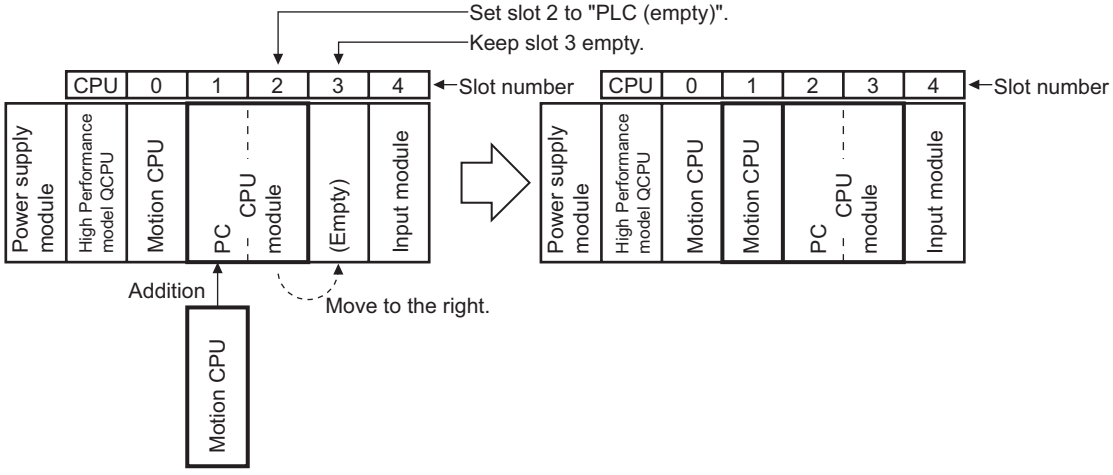
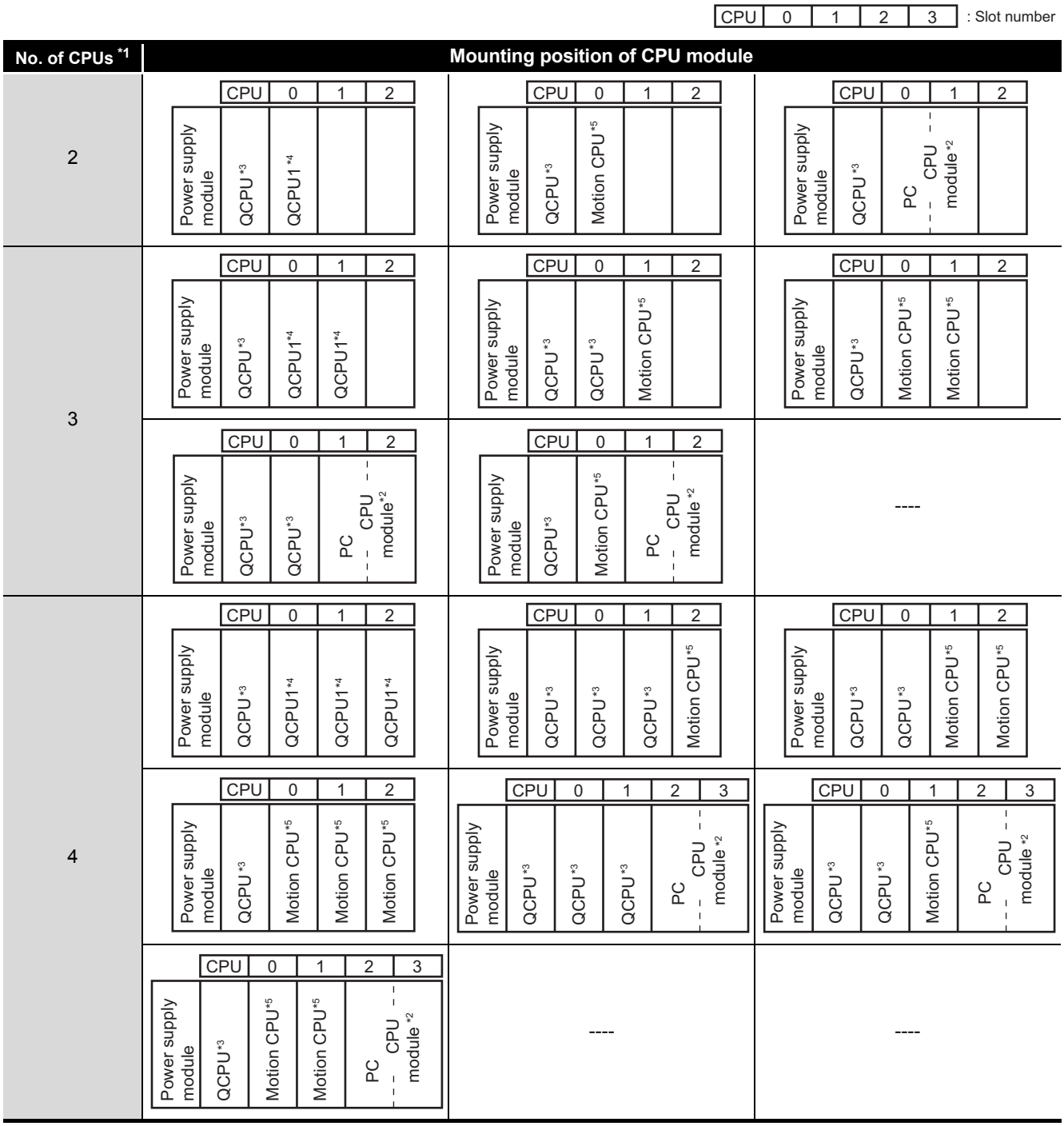


Diagram 3.9 Addition of Motion CPU when PC CPU module is mounted

Table3.3 Mounting position of CPU module



* 1: The number of CPUs shows the value set by the multiple CPU setting.
* 2: The PC CPU module occupies two slots.
* 3: The High Performance model QCPU and Process CPU can be mounted.
* 4: The High Performance model QCPU, Process CPU, and Universal model QCPU (except Q02UCPU) can be mounted.
* 5: The Q172CPUN, Q173CPUN, Q172HCPU, and Q173HCPU can be mounted.

3.1.3 When CPU No.1 is Universal model QCPU

The mounting position of each CPU module is shown is Table3.4.

(1) Mounting position of Universal model QCPU

Only one Q02UCPU can be mounted on the CPU slot (the right side slot of the power supply module).
As for other than Q02UCPU, up to four modules can be mounted from the CPU slot (the right side slot of the power supply module) to slot 2 of the main base unit.

(2) Mounting position of High Performance model QCPU and Process CPU

The High Performance model QCPU or the Process CPU cannot be mounted when the Q02UCPU is used as the CPU No.1.
When the Q02UCPU is used, up to three modules (the High Performance model QCPU(s) and/or the Process CPU(s)) can be mounted on slots 0 to 2.

(3) Mounting position of Motion CPU

Only one Motion CPU can be mounted on slot 0 when the Q02UCPU is used.
When other than the Q02UCPU is used, up to three Motion CPUs can be mounted on slots 0 to 2 of the main base module.

(4) Mounting position of PC CPU module

Only one PC CPU module can be mounted on the right side of the other CPU modules.
(No CPU module can be mounted on the right side of the PC CPU module.)

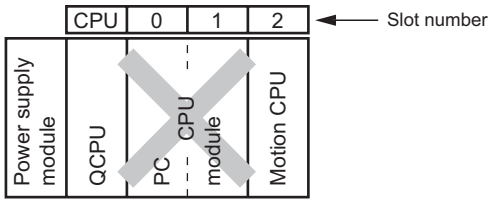


Diagram 3.10 Position where PC CPU module cannot be mounted

Table3.4 Mounting position of CPU module(When the Q02UCPU is mounted on the CPU No.1)

CPU | 0 | 1 | 2 | 3 : Slot number

No. of CPUs *1	Mounting position of CPU module		
2	CPU | 0 | 1 | 2 Power supply module | QnUCPU *2 | Motion CPU *3 | |	CPU | 0 | 1 | 2 Power supply module | QnUCPU*2 | PC - - CPU module*3 - - | |	CPU | 0 | 1 | 2 Power supply module | QnUCPU *2 | PLC (empty) | |
3	CPU | 0 | 1 | 2 Power supply module | QnUCPU*2 | Motion CPU*1 | PC - - CPU module*3 - -	CPU | 0 | 1 | 2 Power supply module | QnUCPU *2 | Motion CPU *3 | PLC (empty)	CPU | 0 | 1 | 2 Power supply module | QnUCPU *2 | PLC (empty) | PLC (empty)
	CPU | 0 | 1 | 2 Power supply module | QnUCPU*2 | PLC (empty) | PC - - CPU module*3 - -	----	----

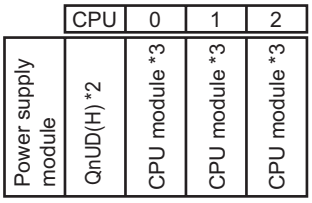
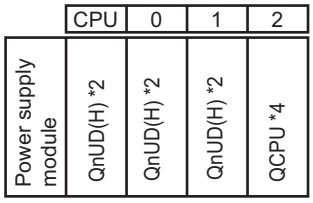
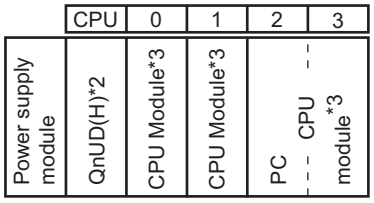
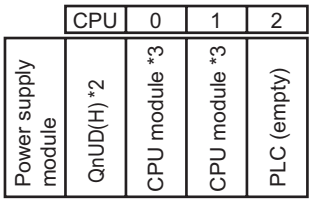
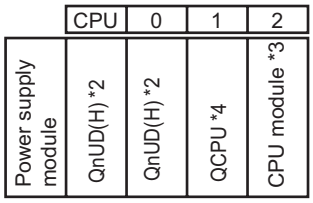
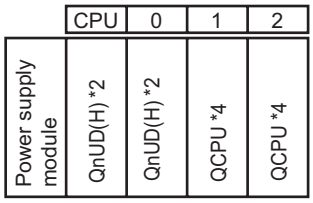
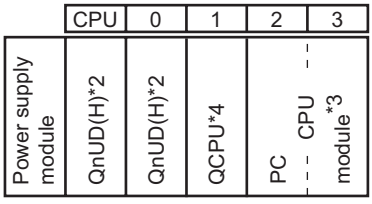
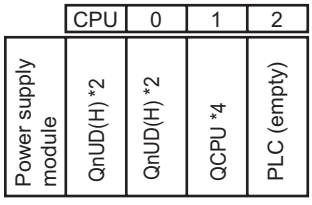
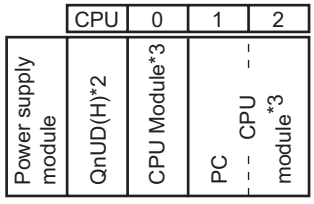
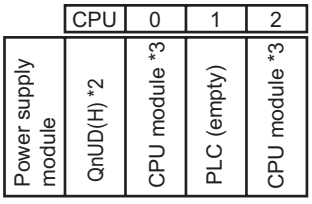
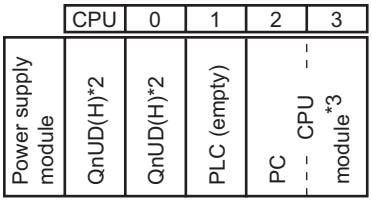
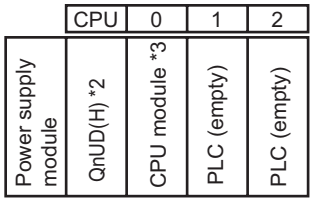
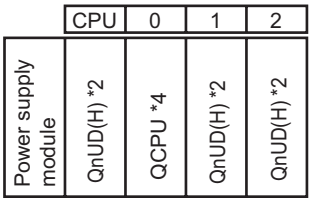
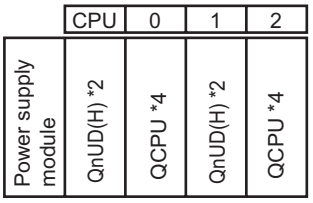
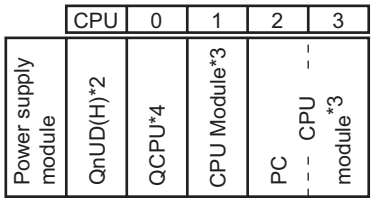
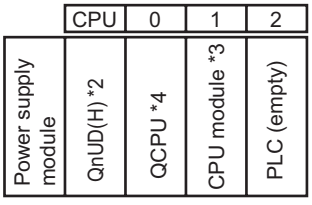
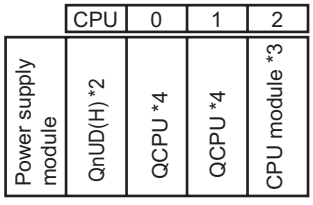
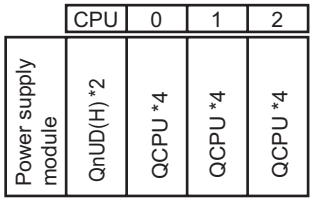
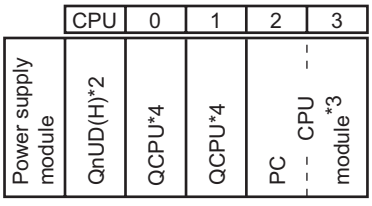
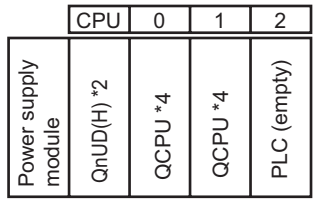
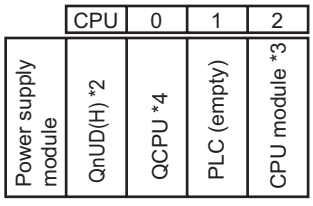
* 1: No. of CPUs indicates the value set in the multiple CPU setting of the PLC parameter.
* 2: The Q02UCPU can be mounted.
* 3: The Q172CPUN, Q173CPUN, Q172HCPU, and Q173HCPU can be mounted.

Table3.5 Mounting position of CPU module(When except the Q02UCPU is mounted on the CPU No.1)

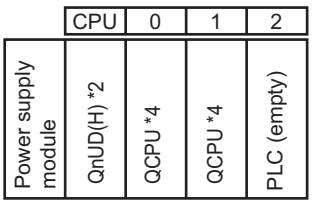
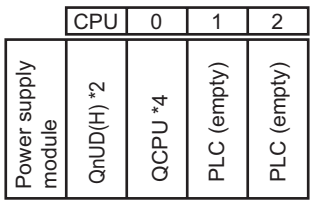
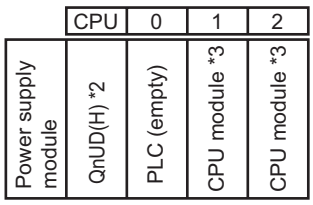
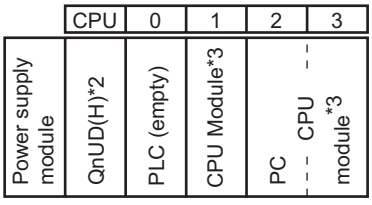
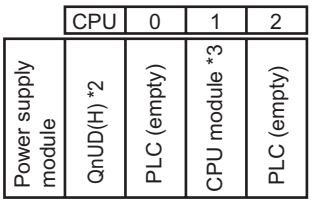
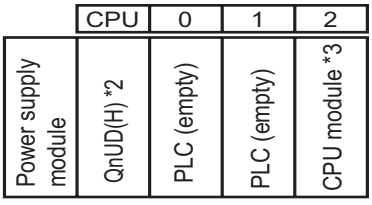
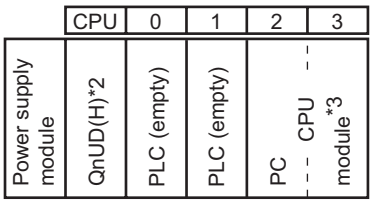
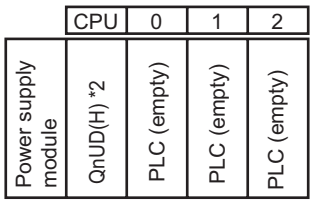
CPU	0	1	2	3	: Slot number

No. of CPUs *1	Mounting position of CPU module		
2	Power supply module / QnUD(H) *2 / CPU module *3	Power supply module / QnUD(H) *2 / QCPU *4	Power supply module / QnUD(H)*2 / PC - - CPU module *3
	Power supply module / QnUD(H) *2 / PLC (empty)	----	----
3	Power supply module / QnUD(H) *2 / CPU module *3 / CPU module *3	Power supply module / QnUD(H) *2 / QnUD(H)CPU *2 / QCPU *4	Power supply module / QnUD(H)*2 / CPU Module*3 / PC - - CPU module *3
	Power supply module / QnUD(H) *2 / CPU module *3 / PLC (empty)	Power supply module / QnUD(H) *2 / QCPU *4 / CPU module *3	Power supply module / QnUD(H)*2 / QCPU*4 / QCPU*4
	Power supply module / QnUD(H)*2 / QCPU*4 / PC - - CPU module *3	Power supply module / QnUD(H) *2 / PLC (empty) / CPU module *3	Power supply module / QnUD(H)*2 / PLC (empty) / PC - - CPU module *3
	Power supply module / QnUD(H) *2 / QCPU *4 / PLC (empty)	Power supply module / QnUD(H) *2 / PLC (empty) / PLC (empty)	----

* 1: No. of CPUs indicates the value set in the multiple CPU setting of the PLC parameter.
* 2: The Q03UDCPU, 04UDHCPU, and Q06UDHCPU can be mounted.
* 3: Universal model QCPU (Q03UDCPU, 04UDHCPU, Q06UDHCPU) and Motion CPU (Q172UDCPU,Q173UDCPU) can be mounted.
* 4: High performance model QCPU and prosess CPU can be mounted.

No. of CPUs *1	Mounting position of CPU module		
4			
			
			
			
			
			
			

* 1: No. of CPUs indicates the value set in the multiple CPU setting of the PLC parameter.
* 2: The Q03UDCPU, 04UDHCPU, and Q06UDHCPU can be mounted.
* 3: Universal model QCPU (Q03UDCPU, 04UDHCPU, Q06UDHCPU) and Motion CPU (Q172UDCPU,Q173UDCPU) can be mounted.
* 4: High performance model QCPU and prosess CPU can be mounted.

No. of CPUs *1	Mounting position of CPU module		
4			
			
			----

* 1: No. of CPUs indicates the value set in the multiple CPU setting of the PLC parameter.
* 2: The Q03UDCPU, 04UDHCPU, and Q06UDHCPU can be mounted.
* 3: Universal model QCPU (Q03UDCPU, 04UDHCPU, Q06UDHCPU) and Motion CPU (Q172UDCPU,Q173UDCPU) can be mounted.
* 4: High performance model QCPU and prosess CPU can be mounted.

3.2 CPU No. of CPU module

(a) CPU No. allocation

Basic
Note3.1

CPU numbers are allocated for identifying the CPU modules mounted on the main base unit in the multiple CPU system. CPU No.1 is allocated to the CPU slot, and CPU No.2, No.3 and No.4 are allocated to the right of the CPU No.1 in this order. *Note3.1*

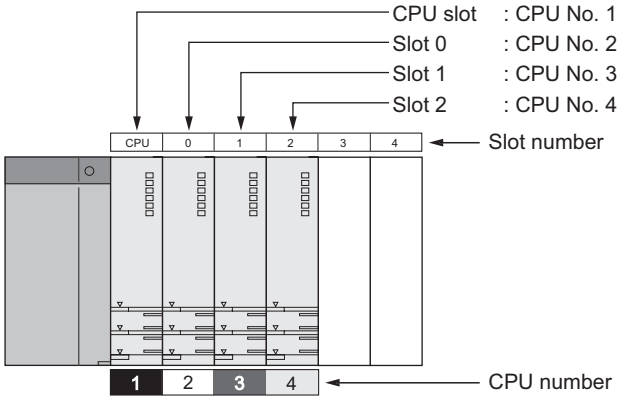


Diagram 3.11 CPU No. allocation

The CPU No. is used for the following applications:

- Specifying the connection target by GX Developer (PC)

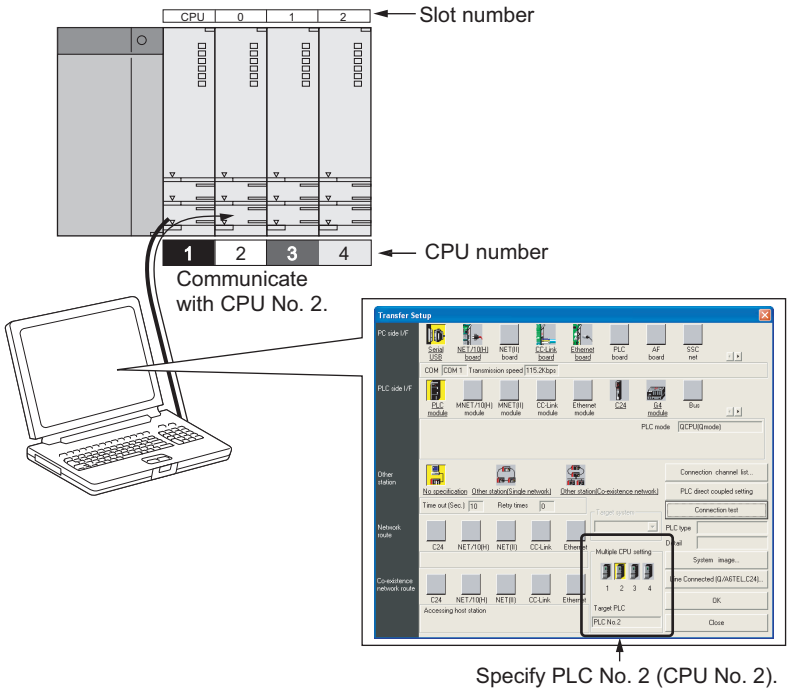


Diagram 3.12 Transfer Setup with GX Developer

Basic
Note3.1

For the Basic Model QCPU, CPU modules can only be mounted up to CPU No. 3. Therefore, CPU No. 4 is not available.

• Setting a control CPU in the I/O assignment.

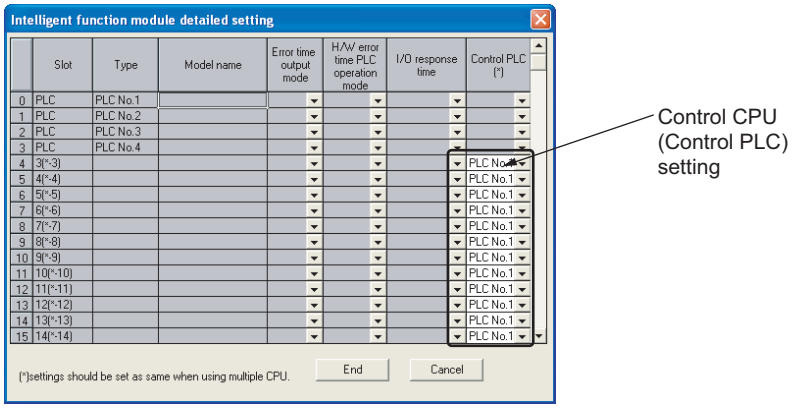


Diagram 3.13 Control CPU setting

(b) Checking host CPU number

The QCPU stores the host number in the special register (SD395).
It is recommended to create a program for checking the host number on the QCPU.
This will enable easy verification when QCPUs are not mounted correctly and when programs are written into other CPUs with GX Developer.

In the program shown in Diagram 3.14, the annunciator (F1) turns to ON when QCPU to which a program is written is other than CPU No.1 (SD395 = 1.)
The "USER" LED on the front of the QCPU is illuminated when the annunciator (F1) turns ON.
The number of the annunciator that has turned ON will be stored in the special register (SD62).

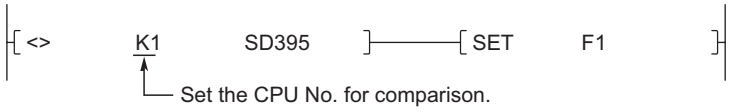


Diagram 3.14 Program for checking host CPU No.

Remark

For the checking of the host CPU number of the Motion CPU or PC CPU module, refer to the relevant manual.

3.3 Concept of I/O number assignment

In the multiple CPU system, I/O numbers are used for interactive transmission between a CPU module and the I/O modules and intelligent function modules, or between CPU modules.

3.3.1 I/O number assignment of each module

The multiple CPU system is different from the Single CPU system in the position (slot) of I/O number 00H.
However, the concept of the order of allocating I/O numbers, I/O numbers for each slot and empty slots is the same for both types.
☞ QCPU User's Manual (Function Explanation, Program Fundamentals)

(1) Position of I/O number "00H"

(a) Slots occupied by CPU modules
The number of slots set with the PLC parameters' multiple CPU settings are occupied by the CPU modules on the multiple CPU system.

(b) Positions of I/O modules and intelligent function modules
I/O modules and intelligent function modules are mounted from the right of the slots occupied by CPU modules.

(c) When not using the PC CPU module
The I/O number for an I/O module or intelligent function module mounted to the next slot to those occupied by CPU modules is set as "00H" and consecutive numbers are then allocated sequentially to the right.
Example: Two CPU modules are mounted

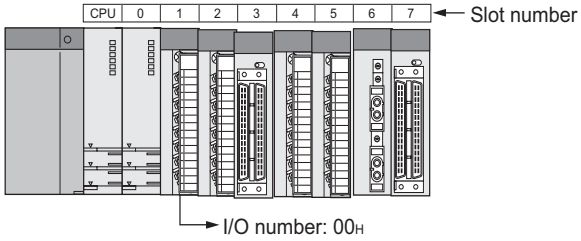


Diagram 3.15 Position of I/O number "00H"

(d) When using the PC CPU module

The PC CPU module occupies two slots. The one on the right side among the two slots is handled as an empty slot. (16 empty points are occupied by default.) Therefore the I/O number of the next slot on the right side of the PC CPU module is "10H." (Set the empty slot to zero point on the I/O assignment of PLC Parameters dialog box, to assign "00H" to the first I/O number.)

(Example) When "No. of CPUs" is set to 3.

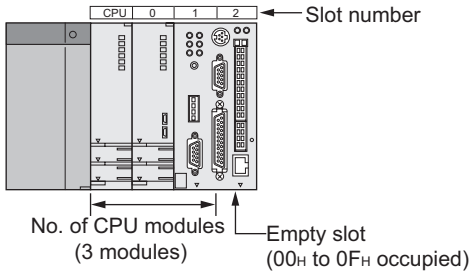


Diagram 3.16 Position of I/O number "00H"

Remark

1) If the number of CPU modules mounted on the main base unit is less than the number set at the "Multiple CPU setting", set the open slot(s) to "PLC (Empty)".
   For the "PLC (Empty)" setting, refer to "Section 3.1"
2) The I/O numbers for the multiple CPU system can be confirmed with the system monitor.
3) The I/O number "00H" can be placed in any slots with I/O assignment setting of PLC parameter.
   ☞QCPU User's Manual (Function Explanation, Program Fundamentals)

3.3.2 I/O number of each CPU module

In the multiple CPU system, I/O numbers are assigned to each CPU module to specify mounted CPU modules.
The I/O number for each CPU module is fixed to the corresponding slot and cannot be changed in the I/O assignment of the PLC Parameter.
Table3.6 shows the I/O number allocated to each CPU module when the multiple CPU system is composed.

Table3.6 I/O number for each CPU module

Universal Basic Note3.2

CPU module mounting position	CPU slot	Slot 0	Slot 1	Slot 2 *Note3.2*
First I/O number	3E00H	3E10H	3E20H	3E30H

The CPU modules I/O numbers are used in the following cases.

- When making communications between CPU modules*1
- When specifying a target CPU module for communication with MC protocol*2

* 1: Refer to CHAPTER 4 for communication between CPU modules.
* 2: Refer to "Q Corresponding MELSEC Communication Protocol Reference Manual" for access to QCPU with MC protocol.

Universal Basic Note3.2

When the Basic model QCPU, or Universal model QCPU (Q02UCPU) is used, available slot is limited up to slot 1 (3E20H).

3.4 Access range of CPU module and other modules

3.4.1 Access range with controlled module

In the multiple CPU system a CPU can refresh I/O data of its controlled modules and write or read data of the buffer memory of intelligent function modules in the same way as a single CPU system.
(☞ QCPU User's Manual (Function Explanation, Program Fundamentals))

3.4.2 Access range with non-controlled module

CPU modules can obtain input (X) ON/OFF data of non-controlled modules and output (Y) ON/OFF data of CPUs of other No. by the PLC parameter setting.
Therefore, ON/OFF data of input modules, I/O composite module or intelligent function modules controlled by other CPUs can be used as interlocks for the host CPU, and the output status to external equipment being controlled by other CPUs can be confirmed.
Also, the contents of the intelligent function module's buffer memory can be read by non-control CPUs regardless of the PLC parameter setting.

However, it is not possible for non-control CPUs to output ON/OFF data to non-controlled output modules, composite I/O module or intelligent function modules, and to write data to the buffer memory of intelligent function modules.

Table3.7 indicates accessibility to the non-controlled modules in the multiple CPU system.

Table3.7 Access range to non-controlled module

Access target		I/O setting outside of the group	
		Disabled (Not checked)	Enabled (Checked)
Input (X)		×	○
Output (Y)	Read	×	○
	Write	×	×
Buffer memory of intelligent function module	Read	○	○
	Write	×	×

○:Accessible ×:Inaccessible

(1) Loading input (X)

The "I/O sharing when using Multiple CPUs" setting in the PLC parameter's Multiple CPU settings determines whether input can be loaded from input modules and intelligent function modules being controlled by other CPUs.

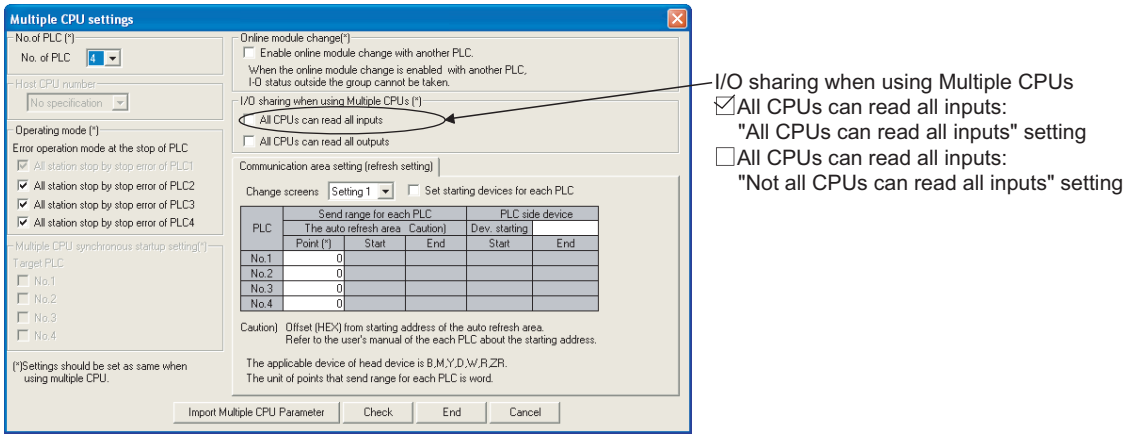


Diagram 3.17 I/O sharing when using Multiple CPUs (input loading)

(a) When "All CPUs can read all inputs" has been set

1) Loads ON/OFF data from the input and intelligent function modules being controlled by the other CPUs by performing input refresh before a sequence program operation starts.
In addition, loading of ON/OFF data from the input and intelligent function modules being controlled by the other CPUs is also available with direct access input (DX).

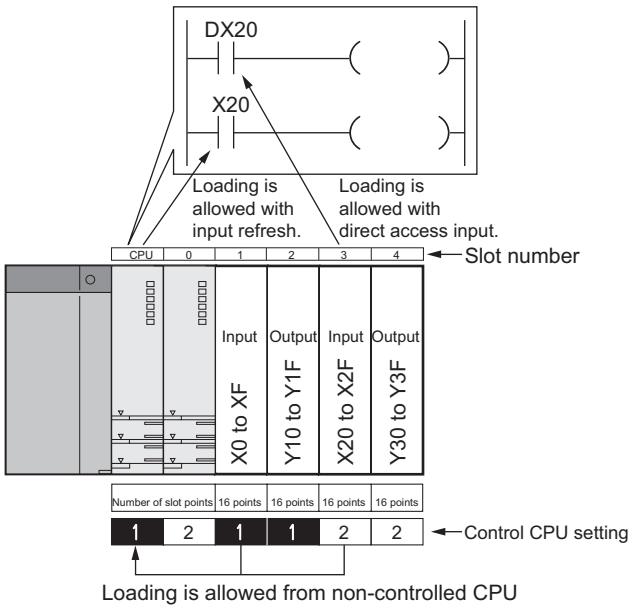


Diagram 3.18 When performing input loading in CPU No.1

2) Input(X) loading is performed for the modules shown in Table3.8, which are mounted to the main base unit or extension base unit(s).

Table3.8 Modules that can load inputs

I/O allocation type	Mounted module
None	Input module
	High speed input module
	I/O composite module*1
	Intelligent function module
Input High speed input I/O mix	Input module
	High speed input module
	Output module*2
	I/O composite module*1
Intelli.	Intelligent function module

* 1: When input(X) loading is performed for QX48Y57 of I/O composite module, input(X) is loaded as all points OFF in Xn8 to XnF assigned to output part.

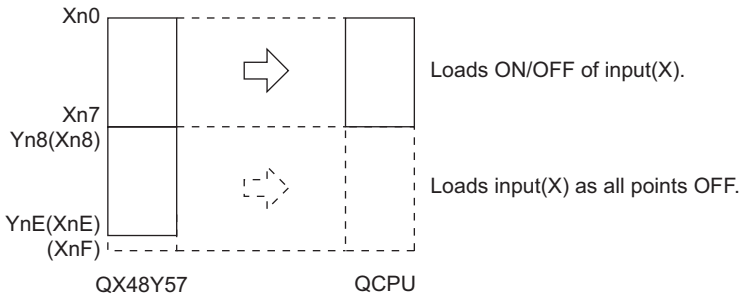


Diagram 3.19 Loading of input(X) from QX48Y57

* 2: When input(X) loading is performed for output module, input(X) is loaded as all points OFF.

3) Input data cannot be loaded from empty slots and remote stations on MELSECNET/H or CC-Link networks being controlled by the other CPU. Use auto refresh of CPU shared memory to use the ON/OFF input data for remote stations on MELSECNET/H or CC-Link in non-controlled CPU.

(b) When "Not all CPUs can read all Inputs" has been set

It is not possible to loads ON/OFF data from input modules and intelligent function modules being controlled by other CPUs (remains at OFF.)

(2) Loading output (Y)

The "I/O sharing when using Multiple CPUs" setting in the PLC parameter's Multiple CPU settings determines whether output can be loaded from output modules and intelligent function modules being controlled by other CPUs.

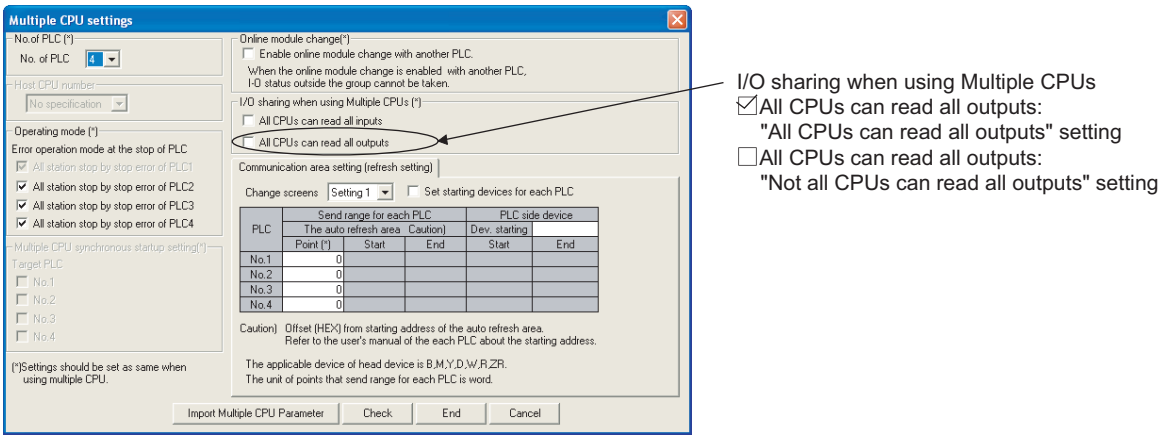


Diagram 3.20 I/O sharing when using Multiple CPUs (output loading)

(a) When "All CPUs can read all outputs" has been set

1) Loads to the host CPU's output (Y) the ON/OFF data that is output to the output module and intelligent function modules being controlled by the other CPUs, by performing output refresh before a sequence program operation starts.

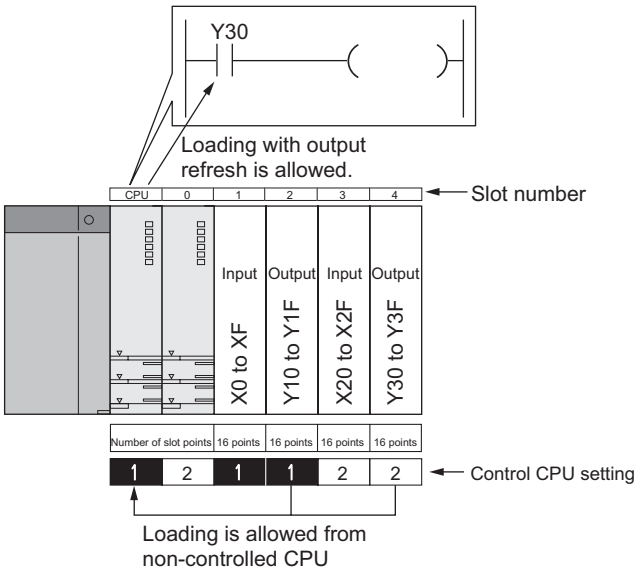


Diagram 3.21 When performing output loading in CPU No.1

2) Output(Y) loading is performed for the modules shown in Table3.9, which are mounted to the main base unit or extension base unit(s).

Table3.9 Modules that can load outputs

I/O allocation type	Mounted module
None	Output module
	I/O composite module
	Intelligent function module
Output I/O mix	Input module
	Output module
	I/O composite module
Intelli.	Intelligent function module

3) Output data cannot be loaded from empty slots and remote stations on MELSECNET/H or CC-Link networks being controlled by the other CPU.
Use auto refresh of CPU shared memory and send the ON/OFF output data for remote stations from control CPU to non-controlled CPU to use the ON/OFF output data for remote stations on MELSECNET/H or CC-Link in non-controlled CPU.

(b) When "Not all CPUs can read all outputs" has been set

It is not possible to load ON/OFF data output to output modules and intelligent function modules by other PLCs into the host CPU's output (Y) (remains at OFF.)

(3) Output to output modules and intelligent function modules

It is not possible to output ON/OFF data to non-controlled modules.
Devices will be turned ON or OFF inside the QCPU when the output from output modules or intelligent function modules controlled by other CPUs is turned ON/OFF by a sequence program, but this will not be actually output to the output modules or intelligent function modules.

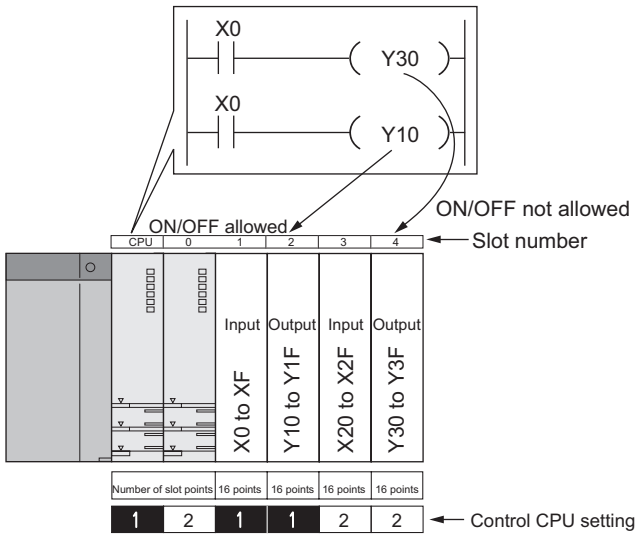


Diagram 3.22 When performing output from CPU No.1 to module

(4) Accessing the intelligent function module buffer memory

(a) Reading from buffer memory

It is possible to read data from the buffer memory of intelligent function modules being controlled by other CPUs with the instructions listed below.

- FROM instruction
- Instructions that use inteligent function module device (U□\G□)

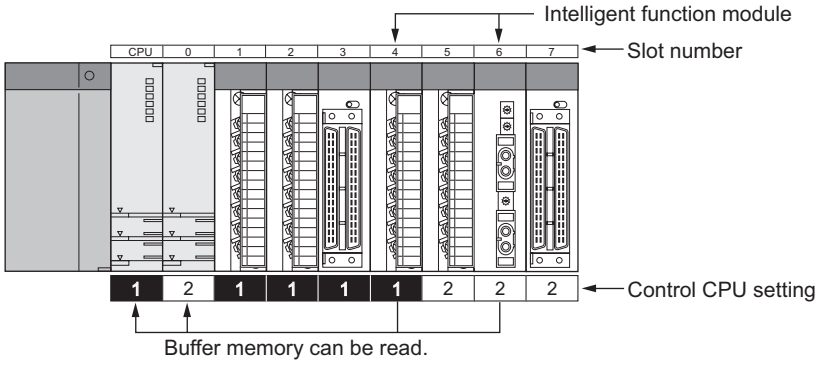


Diagram 3.23 Reading from intelligent function module

(b) Writing to buffer memory

The following instructions cannot be used to write data to the buffer memory of intelligent function modules being controlled by other CPUs.

- TO instruction
- Instructions that use inteligent function module device (U□\G□)
- Intelligent function modules dedicated instructions

An "SP. UNIT ERROR (error code: 2116)" will be triggered if an attempt to write to the intelligent function module controlled by other CPU is carried out.

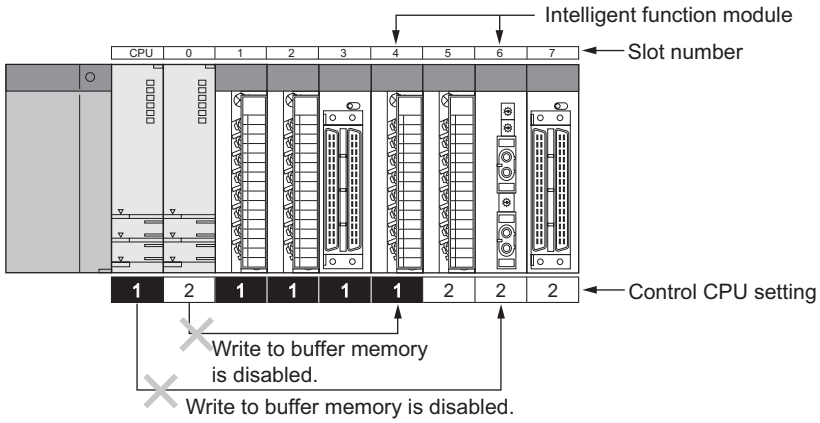


Diagram 3.24 Writing to intelligent function module

3.5 Access target under GOT connection

When a GOT is connected, the access range to QCPU varies depending on the connection method.
For details, refer to the GOT manual.

3.6 Access with instruction using link direct device

Only control CPUs can execute instructions using link direct devices to access other modules.
Link direct devices are not usable for modules being controlled by other CPUs.
"OPERATION ERROR (error code: 4102)" occurs if an instruction using link direct devices is executed to a module controlled by other CPU.

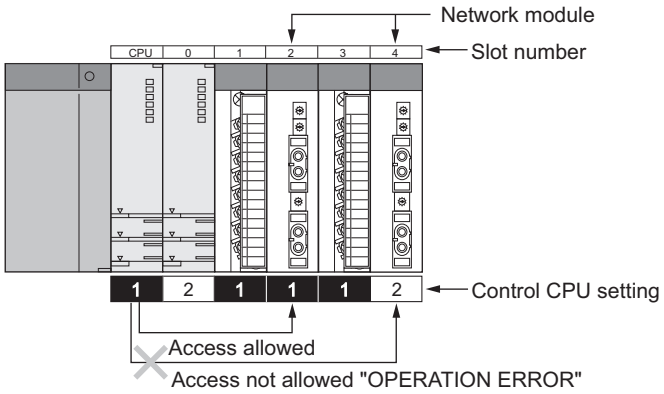


Diagram 3.25 Access with instruction using link direct device

3.7 Access range of GX Developer

(1) Access to QCPU

It is possible to write parameters and programs and perform monitoring and tests on QCPUs connected to GX Developer.

To access QCPUs of other CPU No. via a QCPU connected to GX Developer, specify the target CPU No. in the mulple CPU setting of the GX Developer.

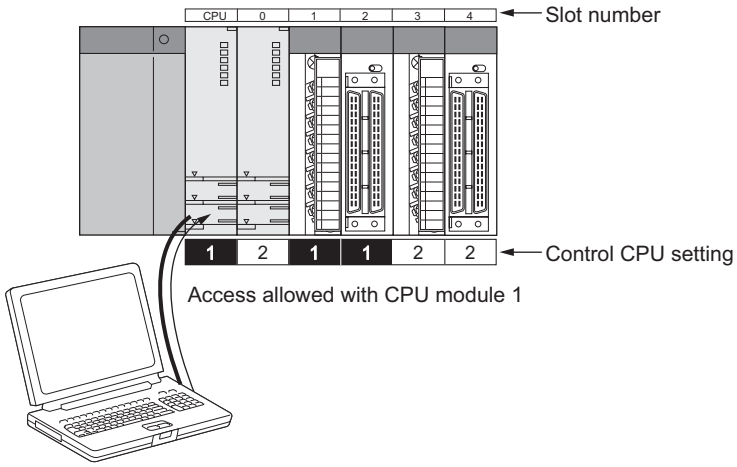


Diagram 3.26 Access to QCPU (when target CPU is not specified)

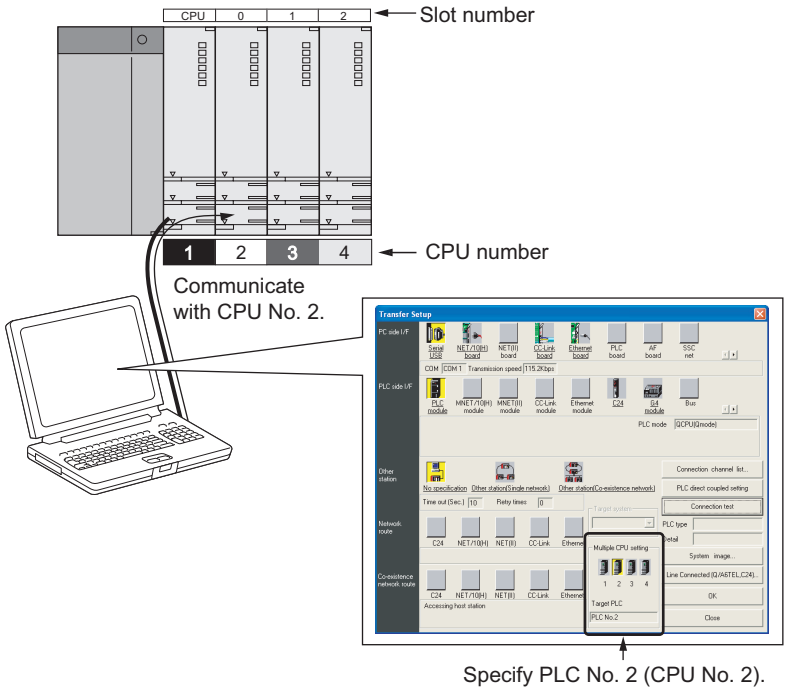


Diagram 3.27 Access to QCPU (when target CPU is specified)

(2) Access to controlled module and non-controlled module

GX Developer can access the modules regardless of whether they are controlled or non-controlled by the QCPU connected to the GX Developr.
By connecting GX Developer to a single QCPU, it is possible to perform monitoring and tests on all modules being controlled by the multiple CPU system's QCPU.
Other station QCPUs on the same MELSECNET/H, Ethernet or other network can also be accessed.

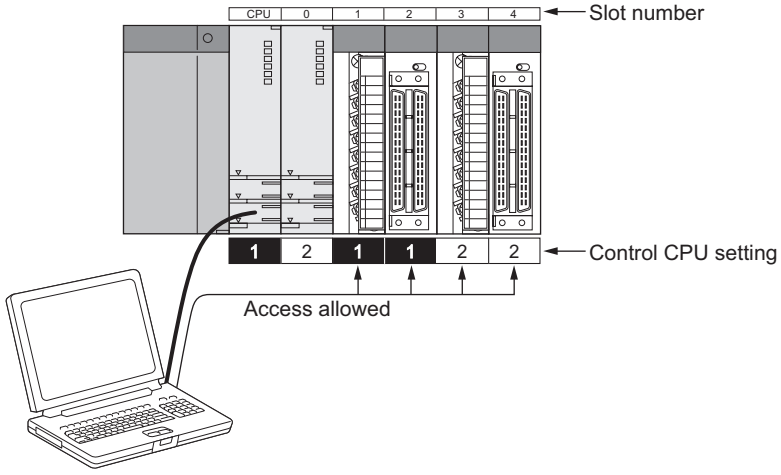


Diagram 3.28 Access to controlled module and non-controlled module

(3) Access from GX Developer in other station

From GX Developer connected to other station on the same network, all QCPUs in the multiple CPU system can be accessed.

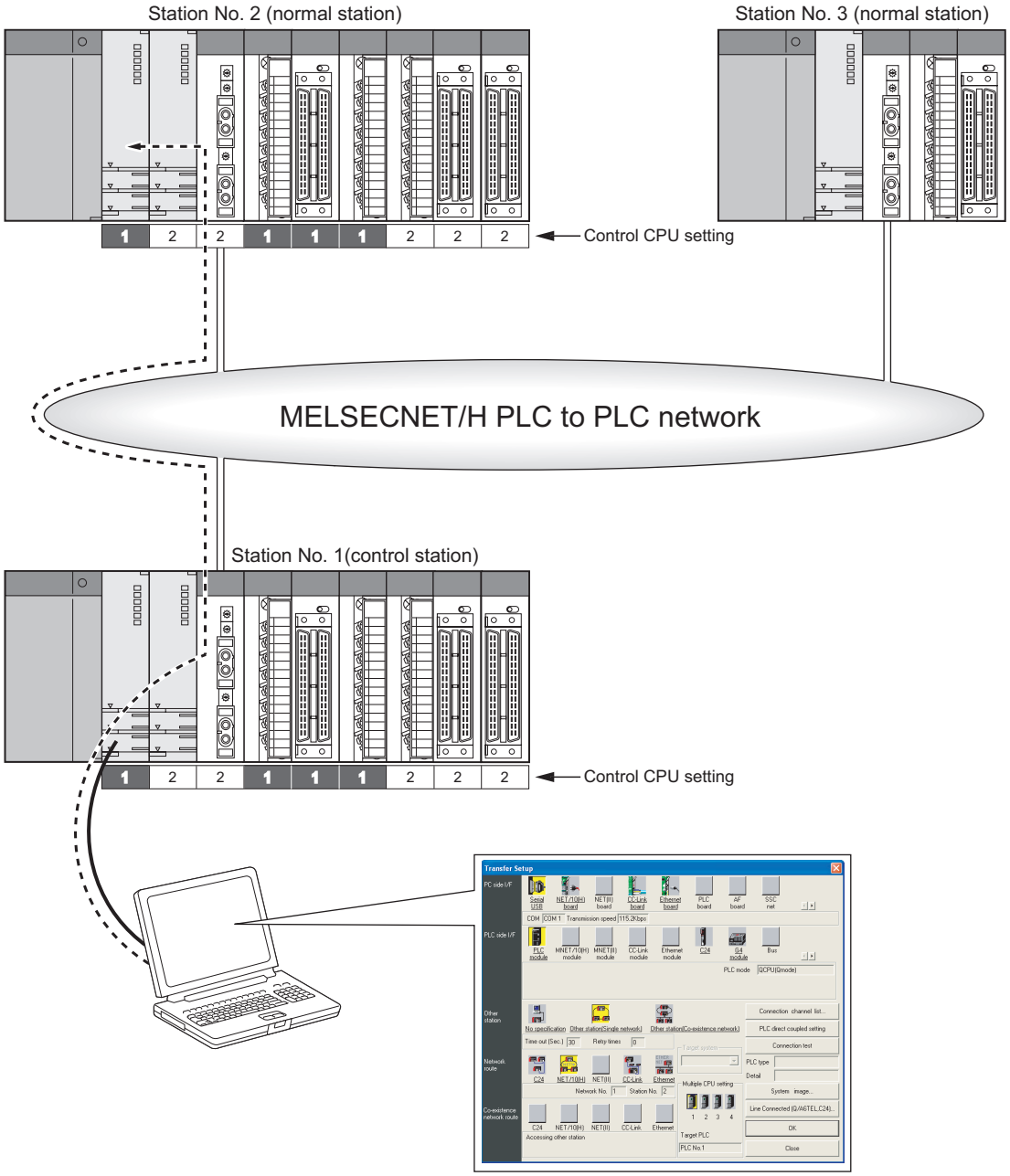


Diagram 3.29 Access through MELSECNET/H PLC to PLC network

3.8 Clock data used by CPU module and intelligent function module

This section shows the clock data used by the CPU module and the intelligent function module.

3.8.1 Clock data used by CPU module

Basic / High Performance / Process Note3.3 / Universal UD Note3.4

The following shows the clock data used by the CPU module.

(1) Setting of clock data

The clock data set to the CPU module No.1 is set to the CPU modules other than the CPU module No.1.
When setting the clock data to the CPU modules other than the CPU module No.1, the clock data of the CPU module No.1 is automatically set to them.

(2) Transmission of clock data

The CPU module No.1 sends the clock data to other CPU modules at the following timing.

The clock data to be sent are year, month, day, day of week, time, minute and second.

- At power-on of Multiple CPU system
- When turing Multiple CPU system from RESET/STOP to RUN
- At 1-second interval after starting up Multiple CPU system

POINT

Since the CPU module No.1 sets the clock data at 1-second interval, error up to 1 second occurs to the clock data of CPU modules other than the CPU module No.1.

3.8.2 Clock data used by intelligent function module

Some intelligent function modules store an error code and time (clock data read from QCPU) into the buffer memory when an error occurs.

The CPU No.1 time data will be stored as the time for the error regardless of whether the module concerned is a control CPU or a non-control CPU.

Basic / High Performance / Process Note3.3

When Basic model QCPU, High Performance model QCPU and Process CPU are used, clock data of CPU No.1 is not set to the other CPU modules.)
Set the clock data to each CPU module.

Universal UD Note3.4

Since the Q02UCPU cannot use the Motion CPU (Q172CPUN, Q173CPUN, Q172HCPU, and Q173HCPU) as CPUs No.2 and No.3, the clock data of the Q02UCPU is not set to the other CPU modules. Set the clock data to each CPU module.Set the clock data to each CPU module.

3.9 Resetting the multiple CPU system

The entire multiple CPU system can be reset by resetting CPU No.1.
The CPU modules of No.2 to No.4, I/O modules and intelligent function modules will be reset when CPU No.1 is reset.

If a stop error occurs in any of the CPUs on the multiple CPU system, either reset CPU No.1 or restart the multiple CPU system (power supply ON→OFF→ON) for recovery.

Recovery is not allowed by resetting the error-stopped CPU modules other than CPU No.1.
(Example) For High Performance model QCPU or Process CPU

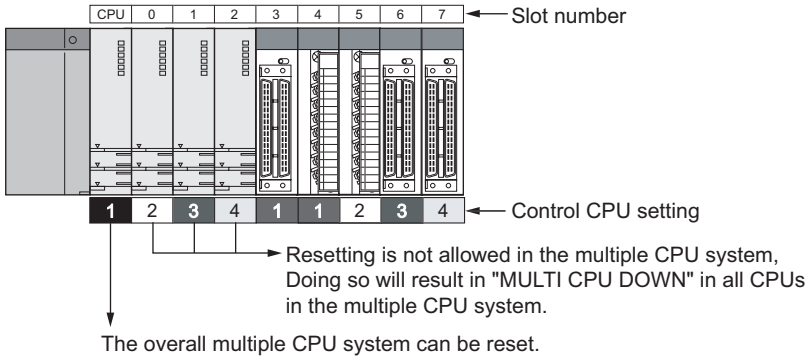


Diagram 3.30 Resetting of multiple CPU system

POINT

(1) It is not possible to reset the CPU modules of No.2 to No.4 individually in the multiple CPU system.
If an attempt to reset any of those CPU modules during operation of the multiple CPU system, a "MULTI CPU DOWN (error code: 7000)" error will occur for the other CPUs, and the entire multiple CPU system will be halted. However, depending on the timing in which any of CPU modules other than No.1 has been reset, an error other than the "MULTI CPU DOWN" may halt the other CPUs.

(2) A "MULTI CPU DOWN (error code: 7000)" error will occur regardless of the operation mode(All stop by stop error of CPU "n"/continue)station set at the "Multiple CPU settings" screen within the "(PLC) Parameter" dialog box when any of CPU modules of No.2 to No.4 is reset (Refer to Section 14.2.8 for details on the multiple CPU setting operation modes.)(☞ Section 3.10)

3.10 Operation for CPU module stop error

The entire system will behaves differently depending whether a stop error occurs in CPU No.1 or any of CPU No.2 to No.4 in the multiple CPU system.

(1) When a stop error occurs at CPU No.1

A "MULTI CPU DOWN (error code: 7000)" error occurs at the other CPUs and the multiple CPU system will be halted when a stop error occurs at the CPU No.1 (☞ Point on the next page for details)

(2) When a stop error occurs at CPU other than No.1

Whether the entire system is halted or not is determined by the multiple CPU setting's "Operating Mode" setting when a stop error occurs in a CPU other than CPU No.1.
The default is set for all CPUs to be stopped with a stop error.
When you do not want to stop all CPUs at occurrence of a stop error in a specific CPU module, remove the check mark that corresponds to the CPU No. so that its error will not stop all CPUs.

Operation mode
☑All station stop by stop error of PLC 'n':
"All station stop by stop error of PLC 'n'" setting
☐All station stop by stop error of PLC 'n':
"Not all station stop by stop error of PLC 'n'" setting

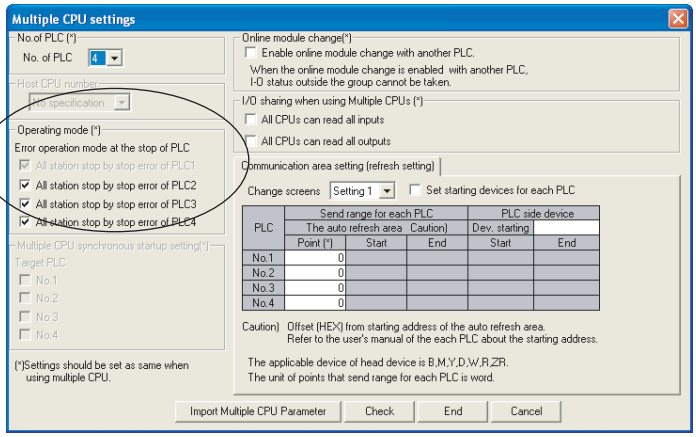


Diagram 3.31 Operation setting for stop error

(a) When "All station stop by stop error of CPU 'n'" is set

When a stop error occurs in the CPU module for which "All station stop by stop error of CPU 'n' " has been set, a "MULTI CPU DOWN (error code: 7000)" error occurs for the other CPU modules and the multiple CPU system will be halted. (☞ POINT on the next page for details.)

(b) When "Not all station stop by stop error of CPU 'n'" is set

When a stop error occurs in the CPU module for which " All station stop by stop error of CPU 'n' " has not been set, a "MULTI EXE. ERROR (error code: 7010)" error occurs in all other CPUs but operations will continue.

POINT

When a stop error occurs, a "MULTI CPU DOWN (error code : 7000)" stop error will occur at the CPU on which the error was detected.
Depending on the timing of error detection, a "MULTI CPU DOWN" error may be detected in a CPU of "MULTI CPU DOWN" status, not the first CPU on which a stop error occurs.
For example, if a stop error occurs in CPU No.2 and CPU No.3 is halted as a direct consequence of this, CPU No.1 may be halted because of the stop error on CPU No.3 depending on the timing of error detection.

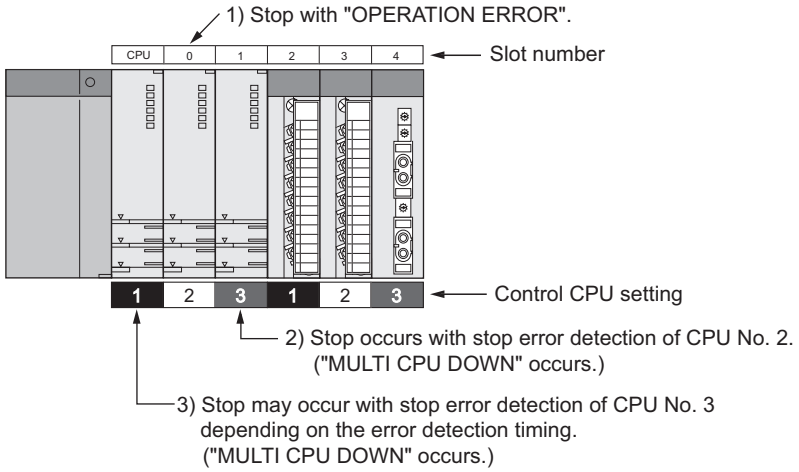


Diagram 3.32 Detection of stop error

Because of this, CPU No. different from the one of initial error CPU may be stored in the error data's common information category.
To restore the system, remove the error cause on the CPU that is stopped by an error other than "MULTI CPU DOWN".
In Diagram 3.33, the cause of the CPU No.2 error that did not cause the "MULTI CPU DOWN" error is to be removed.

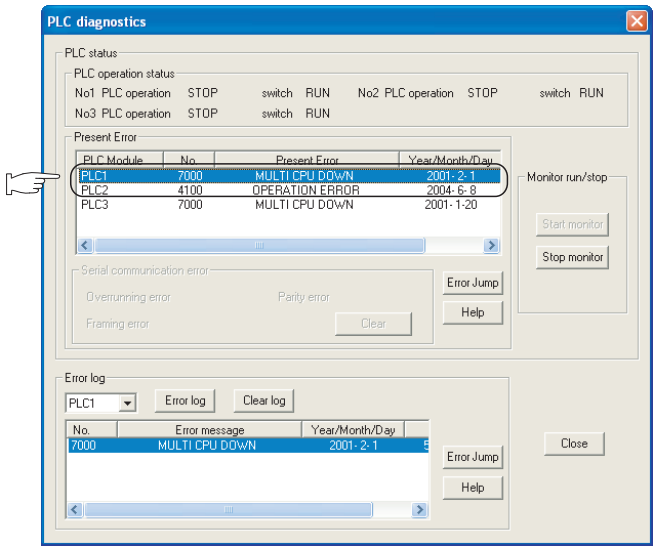


Diagram 3.33 Error display by PLC diagnosis

(3) System recovery procedure

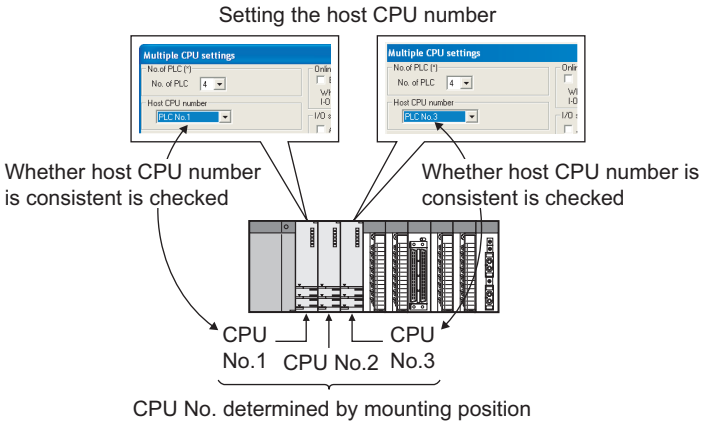
Observe the following procedures to restore the system.

1) Confirm the error-derected CPU No. and error cause with the PLC diagnostics on GX Developer.
2) Remove the error cause.
3) Either reset the CPU No.1 or restart the power to the PLC (power ON→OFF →ON).

All CPUs on the entire multiple CPU system will be reset and the system will be restored when CPU No.1 is reset or the power to the CPU is reapplied.

3.11 Host CPU number of multiple CPU system

Checking the host CPU number of the multiple CPU system is a function to check whether [Host CPU number] in [Multiple CPU settings] of the PLC parameter is identical to the number of the host CPU which is actually mounted. (The number of the host CPU which is actually mounted is determined by the mounting position of the CPU modules.)



POINT

Checking the host CPU number of the multiple CPU system is available when the following CPU modules are used.

- Universal model QCPU (except Q02UCPU)

(1) Setting of checking the host CPU number

When checking the host CPU number of the multiple CPU system, set the CPU number of the CPU module where parameters will be written in [Multiple CPU settings] of the PLC parameter.

The host CPU number is selected from [No specification], [PLC No.1], [PLC No.2], [PLC No.3], and [PLC No.4]. ([No specification] is set by default.)

If [No specification] is set at [Host CPU number], the host CPU number of the multiple CPU system is not checked.

Also, setting the host CPU number is not required for all CPUs.

For example, when the multiple CPU system is configured using three CPUs, the host CPU number can be set to the CPUs No.1 and No.2, and no setting is made to the CPU No.3.

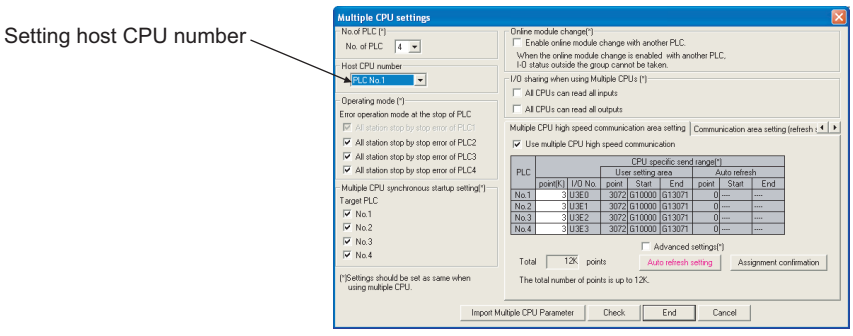


Diagram 3.34 Example of setting host CPU number of multiple CPU system

POINT

When setting the same multiple CPU setting to all the CPU modules that configure the multiple CPU system, set [No specification] at [Host CPU number]. If [No specification] is set at [Host CPU number], all CPU modules used in the multiple CPU system can share the same multiple CPU setting.

(2) Timing of checking host CPU number

The host CPU number of the multiple CPU system is checked when the power supply of the PLC is turned ON or when the CPU module is reset.

If the CPU No. set in the multiple CPU setting is not identical to the CPU No. determined by the mounting position of the CPU modules, "CPU LAY ERROR (error code: 7036)" will occur.

In this case, the Universal model QCPU operates, regarding the CPU No. determined by the mounting position of the CPU modules as correct.

POINT

When the host CPU number is set in [Multiple CPU settings] of the PLC parameter, the direction of auto refresh can be displayed on the auto refresh setting screen using the multiple CPU high speed transmission area.
(The direction of auto refresh can be checked by [Multiple CPU high speed communication area assignment confirmation] screen.)

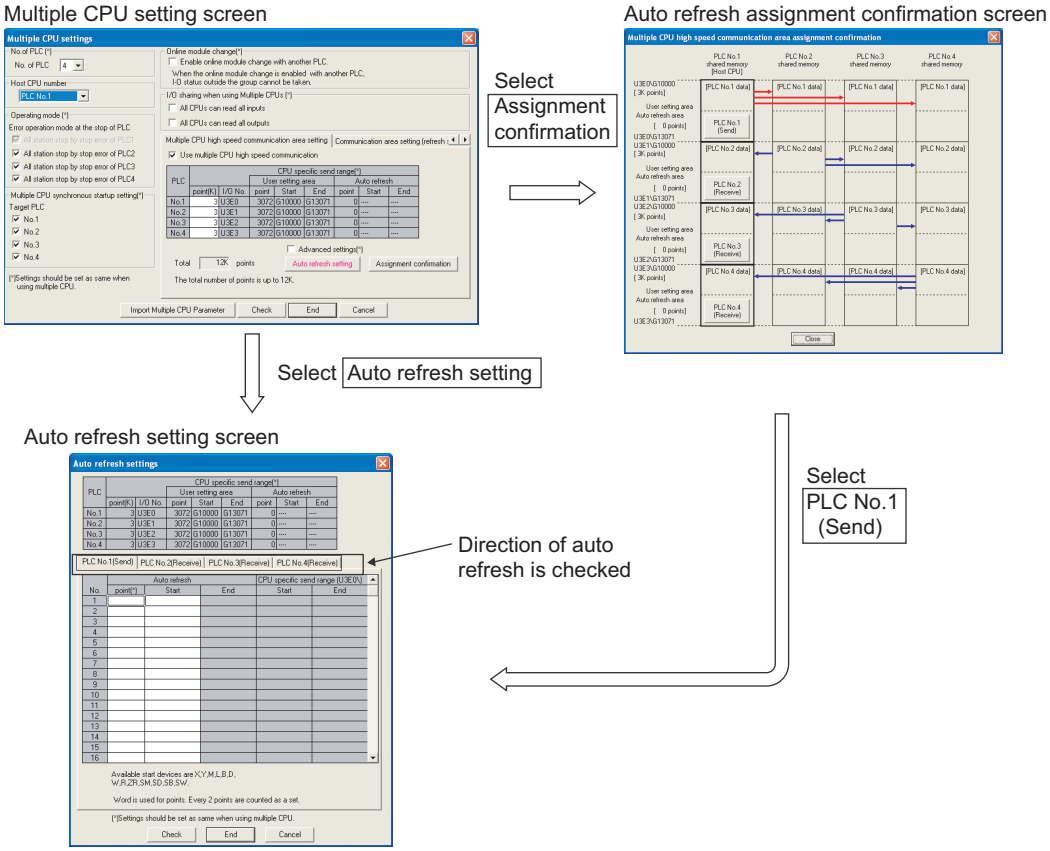


Diagram 3.35 Direction of auto refresh using multiple CPU high speed transmission area

CHAPTER4 COMMUNICATIONS BETWEEN CPU MODULES

In the multiple CPU system, the following methods are available to read/write data between CPU modules:

- Communications with auto refresh
  (☞ Section 4.1.2, Section 4.1.3)
  Data reading/writing between CPU modules
- Communications with programs
  (☞ Section 4.1.4)
  Reading data from or writing data to other QCPU and PC CPU module
- Reading CPU shared memory from QCPU to Motion CPU
- Instructions dedicated to Motion CPU
  (☞ Section 4.2)
  Control instruction from QCPU to Motion CPU with instructions dedicated to Motion CPU
- Instructions dedicated to communication between multiple CPUs
  (☞ Section 4.3)
  Reading or writing of device data from QCPU to Motion CPU
  Event issue from QCPU to Motion CPU, or PC CPU module

(1) Communications between CPU modules

In the multiple CPU system, various communications between CPU modules are available depending on the communication source and destination CPU module types as shown Table4.1.

For communication from the Motion CPU, or PC CPU module, refer to the manual for each CPU module.

Table4.1 Communications between CPU modules

Communication source CPU module	Communication destination CPU module		Communication using CPU shared memory		Using Instructions dedicated to Motion CPU*1	Using instructions dedicated to communication between multiple CPUs
			Auto refresh	By program		
Basic model QCPU	Motion CPU	Q172CPUN Q173CPUN Q172HCPU Q173HCPU	○	○	○	○
	PC CPU module		○	○	×	○
High Performance model QCPU/ Process CPU	High Performance model QCPU/Process CPU/Universal model QCPU		○	○	×	×
	Motion CPU	Q172CPUN Q173CPUN Q172HCPU Q173HCPU	○	○	○	○
	PC CPU module		○	○	×	○
Universal model QCPU	High Performance model QCPU/Process CPU/Universal model QCPU		○	○	×	×
	Motion CPU	Q172DCPU Q173DCPU	○	○	○	○
	PC CPU module		○	○	×	○
Reference			Section 4.1.2 Section 4.1.3	Section 4.1.4	Section 4.2	Section 4.3

○:Available, ×:Not available

* 1: Available instructions are restricted depending on the version of the Motion CPU.

4.1 Communications between CPU modules using CPU shared memory

This chapter describes communication methods between CPU modules of the multiple CPU system using the CPU shared memory.
First, the CPU shared memory is described.

4.1.1 CPU shared memory

The CPU shared memory is a memory provided for each CPU module and by which data are written or read between CPU modules of the multiple CPU system.

The CPU shared memory consists of four areas;

- Host CPU operation information area
- Restricted system area
- Auto refresh area
- User setting area
- Multiple CPU high speed transmission area

The CPU shared memory configuration and the availability of the communication from the host CPU using the CPU shared memory by program are shown in Diagram 4.1 to Diagram 4.3.

• For Basic model QCPU

CPU shared memory			Host CPU		Other CPUs	
			Write	Read	Write	Read
(0H) to (5FH)	0 to 95	Host CPU operation information area	×	○	×	○
(60H) to (BFH)	96 to 191	Restricted system area	×	×	×	○*1
(C0H)	192	Auto refresh area	×	×	×	×
to (1FFH)	to 511	User setting area	○	○	×	○

○: Communication allowed, ×: Communication not allowed

*1: Restricted system area is used for communicating with instructions dedicated to Motion CPU.
Refer to the programming manual of Motion CPU for applications and usage methods of restricted system area used with instructions dedicated to Motion CPU.

Diagram 4.1 Configuration of CPU shared memory

• For High Performance model QCPU or Process CPU

CPU shared memory			Host CPU		Other CPUs	
			Write	Read	Write	Read
(0H) to (1FFH)	0 to 511	Host CPU operation information area	×	×	×	○
(200H) to (7FFH)	512 to 2047	Restricted system area	×	×	×	○*1
(800H)	2048	Auto refresh area	×	×	×	×
to (FFFH)	to 4095	User setting area	○	×	×	○

○: Communication allowed, ×: Communication not allowed

*1: Restricted system area is used for communicating with instructions dedicated to Motion CPU.
Refer to the programming manual of Motion CPU for applications and usage methods of restricted system area used with instructions dedicated to Motion CPU.

Diagram 4.2 Configuration of CPU shared memory

• For Universal model QCPU

		CPU shared memory		Host CPU		Other CPU	
				Write	Read	Write	Read
(0H)	G0	QCPU standard memory	Host CPU operation information area	×	○	×	○
to	to						
(1FFH)	G511						
(200H)	G512		Restricted system area	×	×	×	○
to	to						
(7FFH)	G2047						
(800H)	G2048		Auto refresh area	×	×	×	×
to	to		User setting area	○	○	×	○
(FFFH)	G4095						
(1000H)	G4096	Use-prohibited area*1		×	×	×	×
to	to						
(270FH)	G9999						
(2710H)	G10000	Multiple CPU high speed transmission area*1		○	○	×	○
to	to						
(5F0FH)	Max. G24335						

○: Communication allowed, ×: Communication not allowed

*1: The Q02UCPU does not have the use-prohibited area and the multiple CPU high speed transmission area.

Diagram 4.3 Configuration of CPU shared memory

(1) Host CPU operation information area

(a) Information stored in the host CPU operation information area

The following information is stored in the host CPU operation infomation area in the multiple CPU system.*1

These will all remain as 0 and will not change in the case of single CPU system.

Table4.2 List of host CPU operation information areas

CPU shared memory address	Name	Detail	Description *2	Corresponding special register
0_H	Information availability	Information availability flag	The area to confirm if information is stored in the host CPU's operation information area (1_H to $1F_H$,) or not. • 0: Information not stored in the host CPU's operation information area • 1: Information stored in the host CPU's operation information area	----
1_H	Diagnostic error	Diagnostic error number	An error No. identified during diagnostics is stored in BIN.	SD0
2_H	Time the diagnostic error occurred	Time the diagnosis error occurred	The year and month that the error number was stored in the CPU shared memory's 1_H address is stored with two digits of the BCD code.	SD1
3_H			The day and time that the error number was stored in the CPU shared memory's 1_H address is stored with two digits of the BCD code.	SD2
4_H			The minutes and seconds that the error number was stored in the CPU shared memory's 1_H address is stored with two digits of the BCD code.	SD3
5_H	Error information identification code	Error information identification code	Stores an identification code to determine what error information has been stored in the common error information and individual error information.	SD4
6_H to 10_H	Common error information	Common error information	The common information corresponding to the error number identified during diagnostic is stored.	SD5 to SD15
11_H to $1B_H$	Individual error information	Individual error information	The individual information corresponding to the error number identified during diagnostic is stored.	SD16 to SD26
$1C_H$	Empty	----	Cannot be used	----
$1D_H$	Switch status	CPU switch status	Stores the CPU module switch status.	SD200
$1E_H$	LED status	CPU-LED status	Stores the CPU module's LED bit pattern.	SD201
$1F_H$	CPU operation status	CPU operation status	Stores the CPU module's operation status.	SD203

(b) Reading of host CPU operation information area

Other QCPU can use FROM instruction or multiple CPU area device (U3En\G□) to read data from the host CPU operation information area of the host CPU. However, because there is a delay in data updating, use the read data for monitoring purposes.

* 1: For the Motion CPU, 5_H to $1C_H$ of the host CPU's operation information area is not used. If 5_H to $1C_H$ of the host CPU's operation information area is read from the Motion CPU, it will be read as "0."
* 2: For details, refer to the section describing the corresponding special register in the QCPU User's Manual (Function Explanation, Program Fundamentals).

(2) Restricted system area

The area used by the system of the CPU module (OS.)

(3) Auto refresh area

The area used when the multiple CPU system is automatically refreshed.
(☞ Section 4.1.2)
The points from the address next to the last address in the restricted system area are used for auto refresh.

(4) User setting area

The area for performing communication between CPU modules.
The points after the ones used for the auto refresh area are used.
(An area including the auto refresh area can be used as the user setting area when auto refresh is not performed.)

(5) QCPU standard area

The area provided for the Universal model QCPU to communicate with other CPUs (High Performance QCPU or Process CPU) in a multiple CPU system.
This area includes "Host CPU operation information area", "Restricted system area", "Auto refresh area" and "User setting area".
For each area, refer to (1) to (4).

(6) Multiple CPU high speed transmission area Note4.1

Universal UD Note4.1

The area to perform communication with other CPU modules in the Multiple CPU system using the Universal model QCPU.
The Multiple CPU high speed transmission area has "auto refresh area" and "user setting area."

(a) Auto refresh area

The area used when the Multiple CPU system is automatically refreshed.
(☞ Section 4.1.3)

(b) User setting area

The area for storing data to be sent to other CPU modules by the program.
(☞ Section 4.1.4)
Address for CPU shared memory is 10000 or later.

Universal UD Note4.1

The Q02UCPU cannot perform the communication by the auto refresh using the multiple CPU high speed transmission area.

4.1.2 Communication by auto refresh using CPU shared memory

Universal UD! Note4.2

The following describes communications with auto refresh using auto refresh area in CPU shared memory.Note4.2

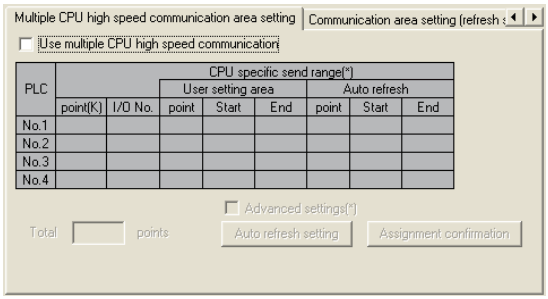
For the communication by the auto refresh using the multiple CPU high speed transmission area in the Universal model QCPUNote4.3, refer to Section 4.1.3.

Universal UD! Note4.3

POINT

In the following case, uncheck Use multiple CPU high speed transmission function of Multiple CPU high speed transmission area setting in the Universal model QCPU.

- The High Performance model QCPU or Process CPU is used as the CPU No.1
- Use multiple CPU high speed transmission function of Multiple CPU high speed transmission area setting in the Universal model QCPU No.1 is unchecked
- The main base unit, slim type main base unit, or redundant power supply base unit is used



Universal UD! Note4.2

For the Universal model QCPU, "auto refresh area of the CPU shared memory" means "auto refresh area of the standard area".
When the Universal model QCPU is used, read this section regarding "CPU shared memory" as "QCPU standard area".

Universal UD! Note4.3

The Q02UCPU cannot perform the communication by the auto refresh using the multiple CPU high speed transmission area.

(1) Communication using auto refresh

(a) Operation of auto refresh

Auto refresh allows communications using the auto refresh area of the CPU shared memory.

By making multiple CPU settings in "PLC parameter", data are automatically written/read between all CPU modules of the multiple CPU system.

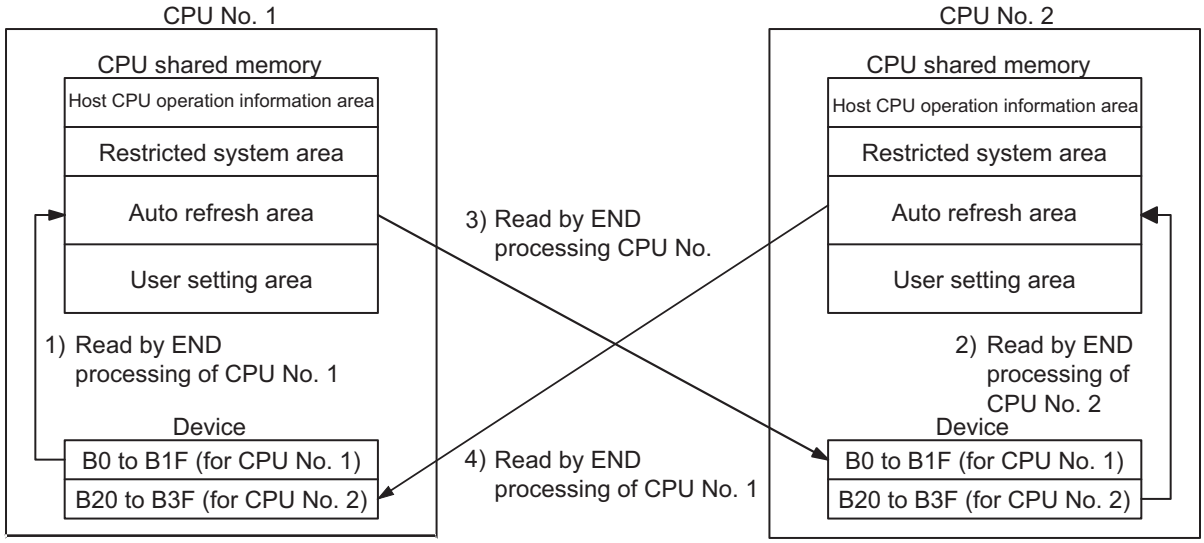
As device memory data of other CPUs are automatically read by the auto refresh function, the host CPU can use those device data.

The following CPU modules in a multiple CPU system can perform auto refresh using auto refresh area in CPU shared memory.

POINT

Auto refresh is a factor for increasing the scan time in the multiple CPU system.
For calculation formulas for the auto refresh time, refer to Section 5.2.

Diagram 4.4 shows an outline of operations when CPU No.1 performs auto refresh of 32 points for B0 to B1F, and when CPU No.2 performs auto refresh of 32 points for B20 to B3F.



The processes performed during CPU No.1 END process.

1): Transfers B0 to B1F transmission device data for CPU No.1 to the host CPU shared memory's auto refresh area.

4): Transfers data in the CPU No.2 CPU shared memory's auto refresh area to B20 to B3F in the host CPU.

The processes performed during CPU No.2 END process.

2): Transfers B20 to B3F transmission device data of CPU No.2 to the CPU shared memory's auto refresh area.

3): Transfers data in CPU No.1 CPU shared memory's auto refresh area to B0 to B1F in CPU No.2.

Diagram 4.4 Operation of auto refresh

(b) Executing auto refresh

Auto refresh is executed when the CPU module is in RUN, STOP or PAUSE status. Auto refresh cannot be performed when a stop error has been triggered in the CPU module.

If a stop error occurs on one module, the other modules without any error will save the data prior to the stop error being triggered.

For example, if a stop error occurs in CPU No.2 when B20 is ON, the B20 in CPU No.1 will remain ON, as shown in the operation outline in Diagram 4.4.

(c) Settings required for auto refresh

When auto refresh is carried out, it is necessary to set the points to be transmitted by each CPU and the device in which the data is to be stored (the device that will perform auto refresh) with the PLC parameter's multiple CPU settings.

(2) Refresh settings

To perform auto refresh in CPU shared memory, set the number of points to be sent from each CPU module (Send range for each PLC) and a device for storing data (PLC side device) on Multiple CPU settings in PLC parameter.

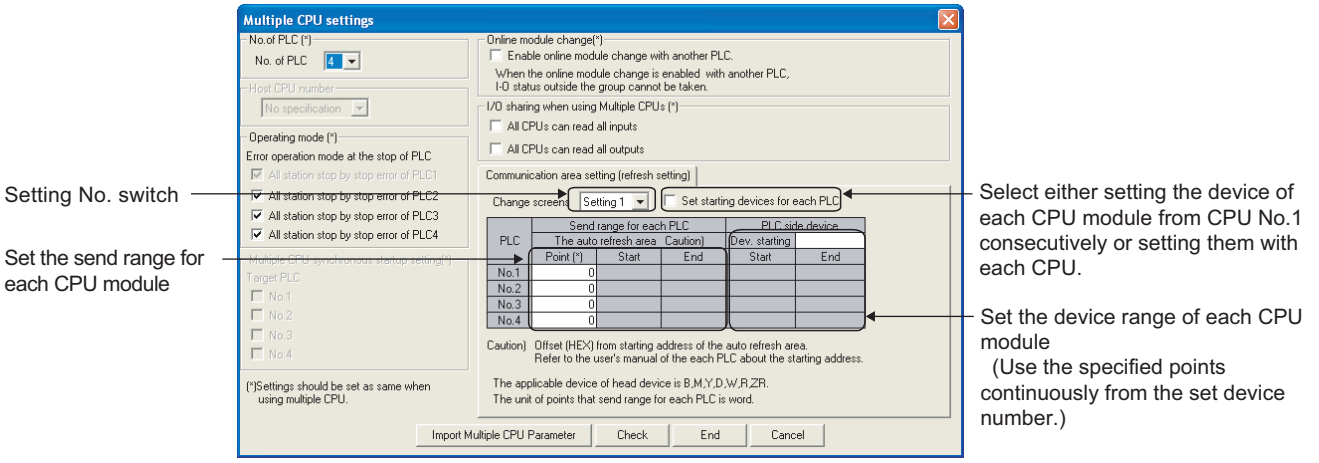


Diagram 4.5 Auto refresh setting screen

(a) Setting switching and send range for each CPU (Refresh range)

1) It is possible to set 4 ranges from Setting 1 to 4 for the refresh setting with the setting switching.
   For example, ON/OFF data can be set to bit devices and other data can be set to word devices separately.

2) In the send range for each CPU, the points of the CPU shared memory are set in 2-point units (2 words.) (2 points in the word device specification and 32 points in the bit device specification)
   Data for which the point is set to "0" in the send range for each CPU will not be refreshed.
   When refresh is performed for 32 points (B0 to B1F) on CPU No.1 and 32 points (B20 to B3F) on CPU No.2, the number of send points is 2 for CPU No.1 and 2 for CPU No.2 since 1 point of the CPU shared memory is equal to 16 points of bit devices.

3) The number of send points is as follows:

• For Basic model QCPU

The numbers of send points are 320 words for the Basic model QCPU and 2048 words for the Motion CPU/PC CPU module, making a total of 4416 points (4416 words) for all CPU modules.

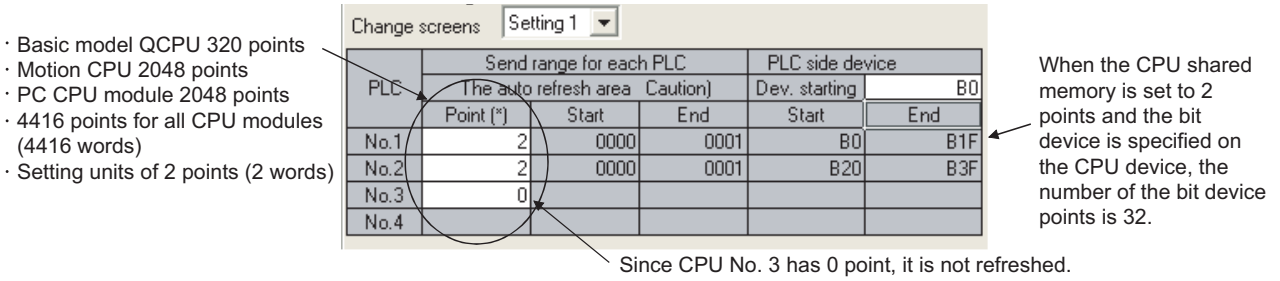


Diagram 4.6 Setting of send points

• For High Performance model QCPU or Process CPU, or Universal model QCPU

The number of send points is a maximum of 2 k points (2 k words) for a total of four ranges for each CPU module, making a total of 8 k points (8 k words) for all CPUs.

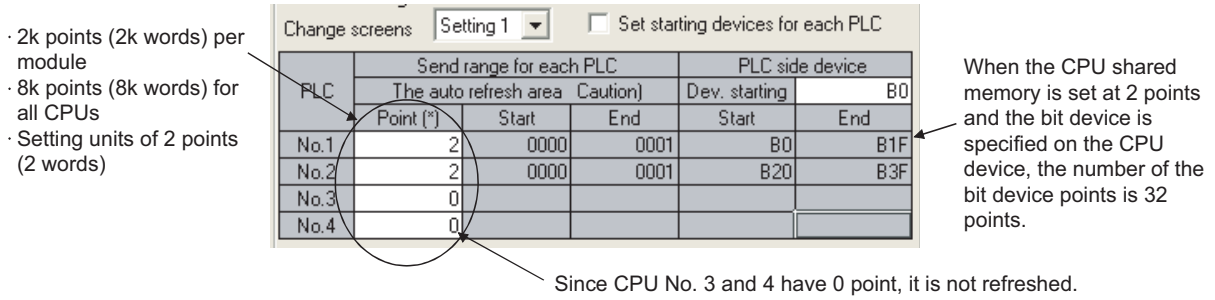


Diagram 4.7 Setting of send points

[Processing of auto refresh]

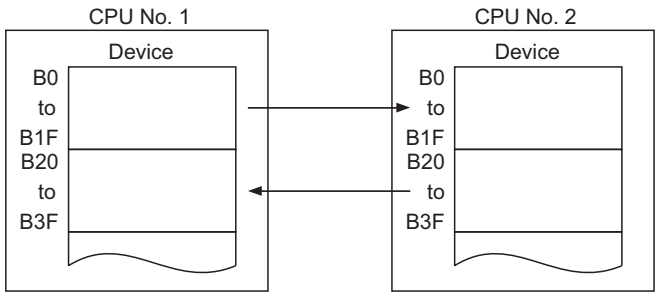


Diagram 4.8 Outline of auto refresh processing (between CPU No. 1 and No. 2)

4) The area occupied for auto refresh in the CPU shared memory is a total of Setting 1 to 4.
When send points are set, the first and last addresses of the auto refresh area are automatically displayed as hexadecimal offset values.
For example, the CPU that has send point setting in Setting 1 and 2 has the last address of "the first address of the auto refresh area + offset value of Setting 2". (In Diagram 4.9, up to "the first address of the auto refresh area + 11_H" are set for CPU No. 1 and 2, and "the first address of the auto refresh area + 21_H" is set for CPU No. 4.)
When a CPU has setting in Setting 1 only, the last address in Setting 1 is the one of the CPU's auto refresh area.

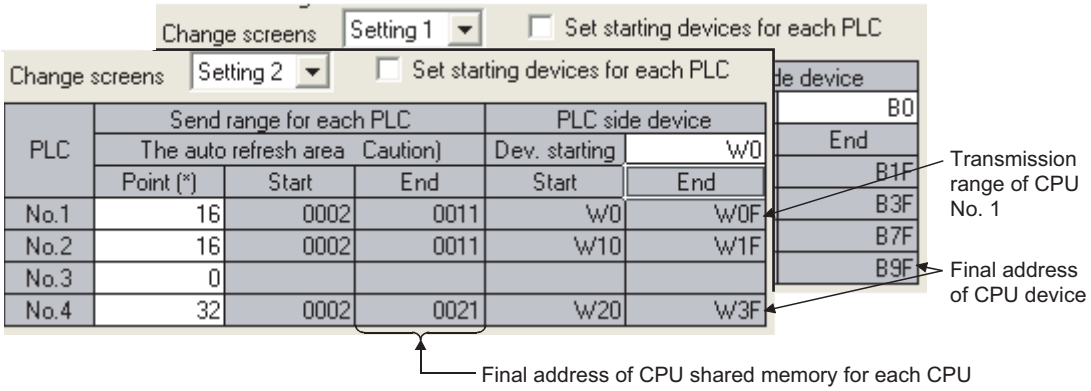


Diagram 4.9 Display of auto refresh area address

5) The same number of send points must be set for all CPUs in the multiple CPU system.
If different number of send points is set for a CPU, "PARAMETER ERROR" occurs in the consistency check between CPUs.
(☞ Section 6.1 (3))
For details of consistency check between CPUs, refer to Section 6.1.

(b) CPU devices

The following devices can be used for auto refresh purposes (other devices cannot be set up with the GX Developer.)

Table4.3 Devices used for auto refresh

Settable devices	Caution
Data register (D) Link register (W) File register (R, ZR)	None
Link relay (B) Internal relay (M) Output (Y)	Specify 0 or multiples of 16 for the first number.

Basic High Performance Process Note4.4

1) For setting the CPU side devices, the following 2 methods are available. *Note4.4*
   - Method of setting devices from the startive device of CPU No.1 consecutively
   - Method of setting devices for each CPU module optionally

Change screens: Setting 1 ☐ Set starting devices for each PLC

PLC	Send range for each PLC			PLC side device	
	The auto refresh area Caution)			Dev. starting	
	Point (*)	Start	End	Start	End
No.1	0				
No.2	0				
No.3	0				
No.4	0				

☐ Set starting devices for each PLC. : Method of setting devices from the startive device of CPU No.1 consecutively
☑ Set starting devices for each PLC. : Method of setting devices for each CPU module optionally

Diagram 4.10 Selection of setting method for the CPU side devices

2) The CPU side devices use the device range of points set for each CPU module from the set startive device.
Set a device number so that the necessary amount of send point devices can be secured.
Sixteen times the number of send points will be set if a bit device is specified in the CPU device.
(Example) If the total number of send points for all CPU modules is 10, then 160 points of B0 to B9F are set when B0 link relay is specified.

Basic High Performance Process Note4.4

For Basic model QCPUs and High Performance model QCPUs/Process CPUs of which the first 5 digits of serial No. is "07031" or earlier, auto refresh is available only by setting devices consecutively from the starting device of CPU No.1.
In addition, when using GX Developer of Version 8.22Y or earlier, auto refresh is also available only by setting devices consecutively from the starting device of CPU No.1.

3) The CPU devices are set as follows.
   - It is possible to change the device for settings 1 to 4.
     The same devices can also be specified as long as the device range for settings 1 to 4 are not overlapped.

Setting 1: For link relay

Change screens: Setting 1 ☐ Set starting devices for each PLC

PLC	Send range for each PLC (The auto refresh area Caution)			PLC side device	
				Dev. starting	B0
	Point (*)	Start	End	Start	End
No.1	2	0000	0001	B0	B1F
No.2	2	0000	0001	B20	B3F
No.3	4	0000	0003	B40	B7F
No.4	2	0000	0001	B80	B9F

Setting 2: For link register

Change screens: Setting 2 ☐ Set starting devices for each PLC

PLC	Send range for each PLC (The auto refresh area Caution)			PLC side device	
				Dev. starting	W0
	Point (*)	Start	End	Start	End
No.1	16	0002	0011	W0	W0F
No.2	16	0002	0011	W10	W1F
No.3	0				
No.4	32	0002	0021	W20	W3F

Setting 3: For link relay

Change screens: Setting 3 ☐ Set starting devices for each PLC

PLC	Send range for each PLC (The auto refresh area Caution)			PLC side device	
				Dev. starting	B100
	Point (*)	Start	End	Start	End
No.1	2	0012	0013	B100	B11F
No.2	2	0012	0013	B120	B13F
No.3	4	0004	0007	B140	B17F
No.4	4	0022	0025	B180	B1BF

The Start and the End addresses are automatically calculated with GX Developer.

- Settings with different devices are available at setting 1 to setting 4.
- The same devices can be set for settings 1 to 4.
- Since 160 points of BO9 to B9F are used in setting 1, BA0 or large value must be entered in setting 3.
  Partially duplicate settings like B0 to B9F for setting 1 and B90 to B10F for setting 3 are not allowed.

Diagram 4.11 Setting of devices at CPU

[Processing of auto refresh]

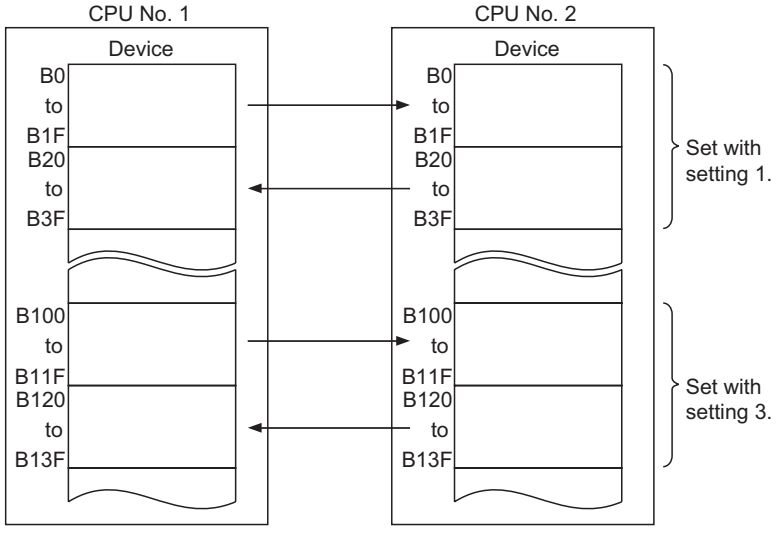


Diagram 4.12 Outline of auto refresh processing (between CPU No. 1 and No. 2)

- Devices of setting 1 to 4 can be set independently for each CPU.
  For example, devices of CPU No.1 can be set up as link relays, and those of CPU No.2 can be set up as internal relays.

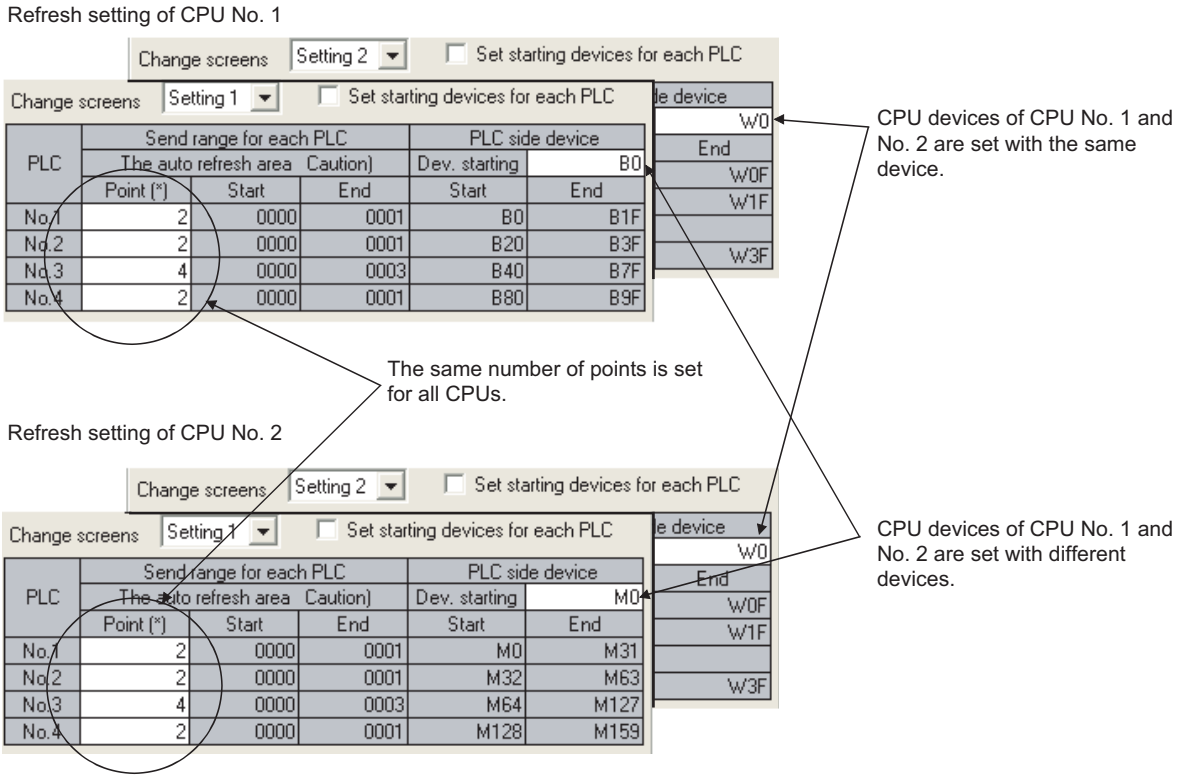


Diagram 4.13 Devices set individually for each CPU

[Processing of auto refresh]

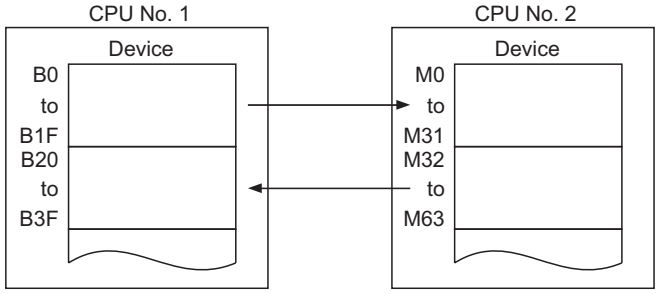


Diagram 4.14 Outline of auto refresh processing (between CPU No. 1 and No. 2)

4) When the auto refresh operations are divided into four ranges (Setting 1: Link relay (B), Setting 2: Link register (W), Setting 3: Data register (D), Setting 4: Internal relay (M)), the outline is as shown in Diagram 4.15.

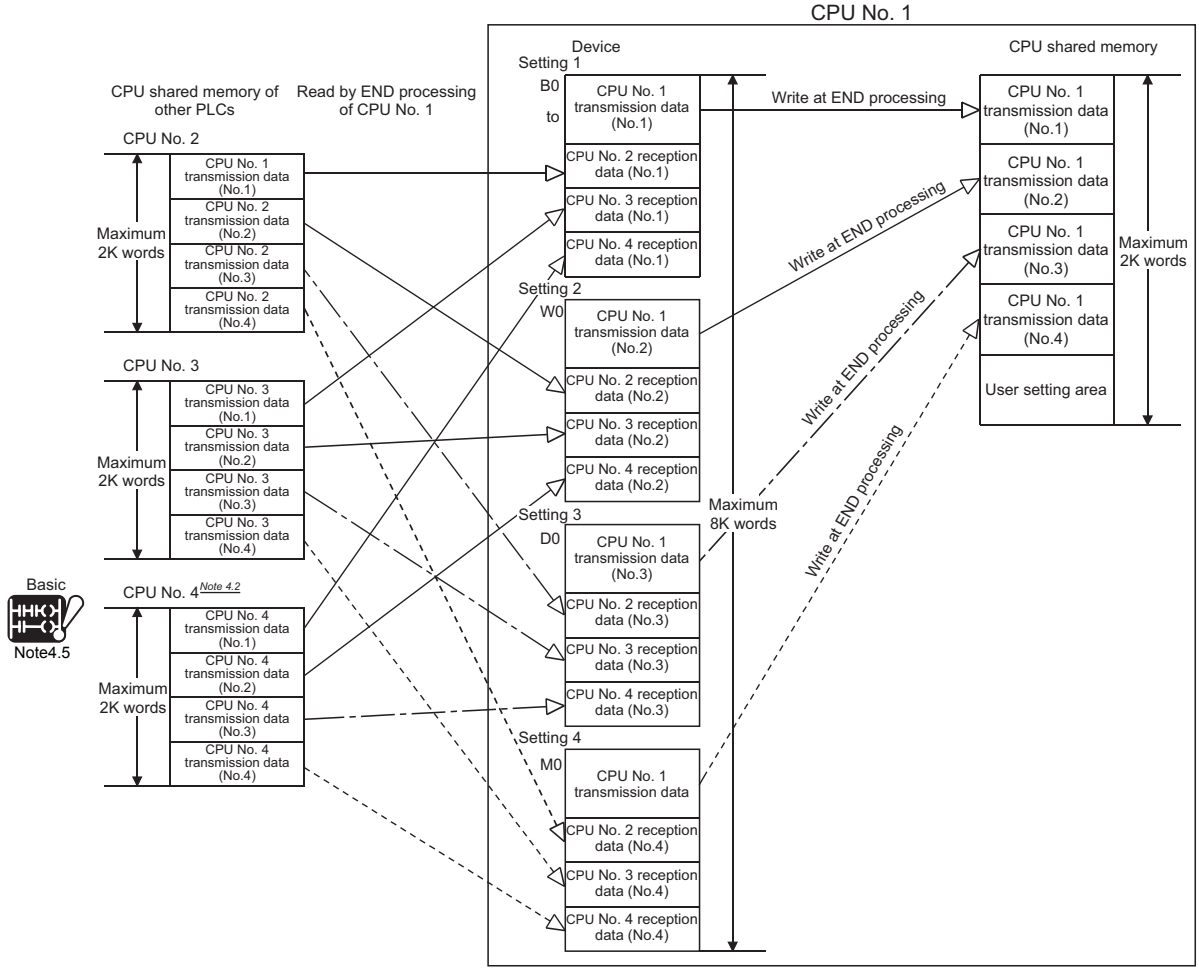


Diagram 4.15 Outline of auto refresh operations using 4 ranges

Basic
Note4.5

Since the number of CPU modules that can be mounted is up to 3 when using the basic model QCPU, there is no CPU No.4.

POINT

The followings are available when selecting the method of setting devices with each CPU optionally.

- The order of the send range for each module can be changed, since devices can be set individually.
- The system scan time can be reduced, since it is possible to set for not performing unnecessary refresh.

(Example 1) When changing the order of send range for each CPU module

The following shows the example performing auto refresh between High Performance model QCPU of CPU No.1 and Motion CPU of CPU No.2.

By setting devices optionally, it is possible to match the device of Performance model QCPU to the fixed device in Motion CPU.

Change screens: Setting 1 — Set starting devices for each PLC

PLC	Send range for each PLC			PLC side device	
	The auto refresh area Caution)			Dev. starting	
	Point (*)	Start	End	Start	End
No.1	48	0000	002F	M3072	M3839
No.2	66	0000	0041	M2000	M3055
No.3					
No.4					

Setting of CPU No.1

Setting 1

CPU	Send range for each CPU			CPU side device	
	CPU share memory G			Dev. starting	*
	Point (*)	Start	End	Start	End
No.1	48	0800	082F	M3072	M3839
No.2	66	0800	0841	M2000	M3055
No.3					
No.4					

Setting of CPU No.2

Diagram 4.16 Setting of CPU device

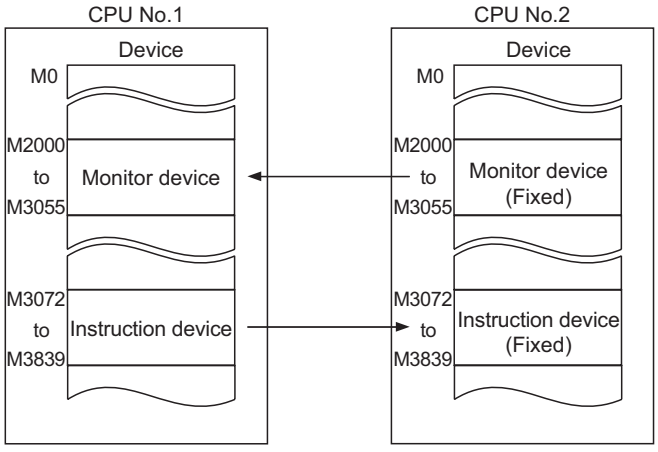


Diagram 4.17 Outline of auto refresh operation

(Example 2) When setting not to perform unnecessary refresh

The following shows the example performing auto refresh between each CPU from No.2 to No.4 and CPU No.1 only.

By leaving the device column of other CPUs of which auto refresh is not required in blank, it is possible to set not to perform unnecessary refresh.

The device column of the host CPU cannot be left in blank.

Change screens: Setting 1 — Set starting devices for each PLC

PLC	Send range for each PLC: The auto refresh area Caution) Point (*)	Start	End	PLC side device: Dev. starting Start	End
No.1	10	0000	0009	D100	D109
No.2	10	0000	0009	D0	D9
No.3	10	0000	0009	D10	D19
No.4	10	0000	0009	D20	D29

Setting of CPU No.1

Change screens: Setting 1 — Set starting devices for each PLC

PLC	Send range for each PLC: The auto refresh area Caution) Point (*)	Start	End	PLC side device: Dev. starting Start	End
No.1	10	0000	0009	D100	D109
No.2	10	0000	0009	D0	D9
No.3	10	0000	0009		
No.4	10	0000	0009		

Setting of CPU No.2

Change screens: Setting 1 — Set starting devices for each PLC

PLC	Send range for each PLC: The auto refresh area Caution) Point (*)	Start	End	PLC side device: Dev. starting Start	End
No.1	10	0000	0009	D100	D109
No.2	10	0000	0009		
No.3	10	0000	0009	D0	D9
No.4	10	0000	0009		

Setting of CPU No.3

Change screens: Setting 1 — Set starting devices for each PLC

PLC	Send range for each PLC: The auto refresh area Caution) Point (*)	Start	End	PLC side device: Dev. starting Start	End
No.1	10	0000	0009	D100	D109
No.2	10	0000	0009		
No.3	10	0000	0009		
No.4	10	0000	0009	D0	D9

Setting of CPU No.4

Diagram 4.18 Setting of CPU device

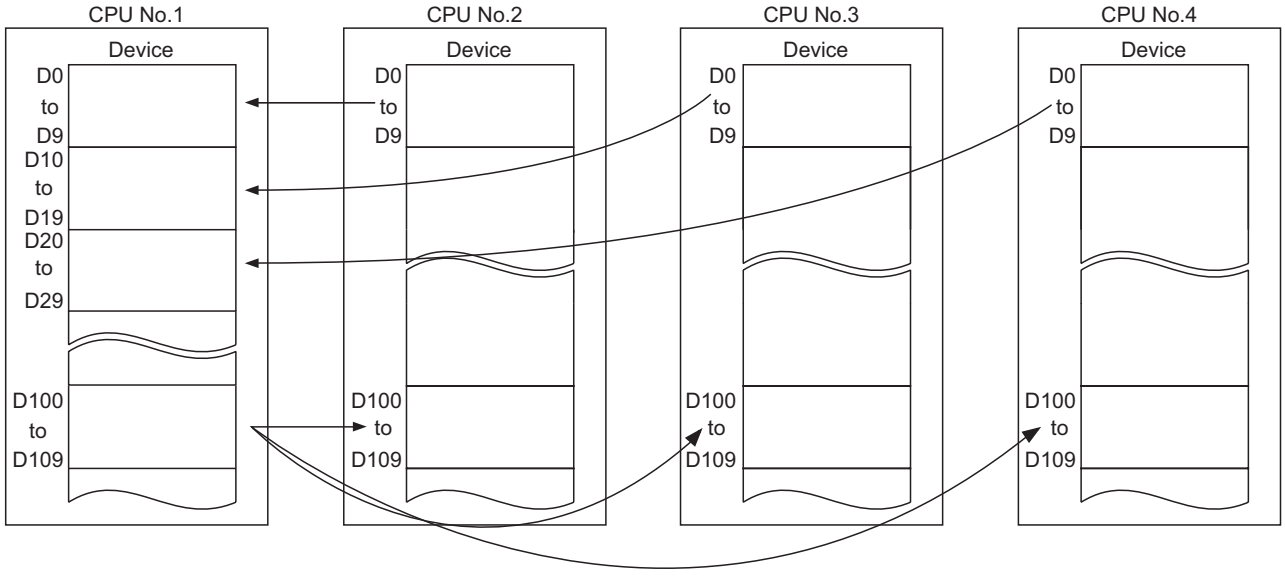


Diagram 4.19 Outline of auto refresh operation

(3) Precautions

Basic Note4.6

(a) Local device setting Note4.6

Device ranges set for the use of the auto refresh cannot be set to local devices.
If set, the refresh data will not be updated.

Basic Note4.7

(b) Setting for using the same file name as the program in the file register Note4.7

Do not set devices for the use of the auto refresh in the file register for each program.
If set, auto refresh will be performed on the file register that corresponds to the last scan execution type program executed.

(c) Assurance of data sent between CPUs

The old data and the new data may be mixed in each CPU due to the timing of sending data from the host CPU and auto refresh in the other CPU.
The following shows the method to realize the data consistency of the user data in the communication by the auto refresh.

1) Data consistency for 32 bit data

Since the data transmission by the auto refresh mode can be set in units of 32 bits only, data separation for 32 bits data will not occur.

Basic Note4.6

The Basic model QCPU does not have any local device.

Basic Note4.7

Since the file register in the Basic model QCPU is fixed, file register cannot be set for each program.

2) Data consistency for data exceeding 32 bits

In auto refresh method, data are read in descending order of the setting number in auto refresh setting parameter.

Read data separation can be avoided by using the setting number lower than the setting data as an interlock device.

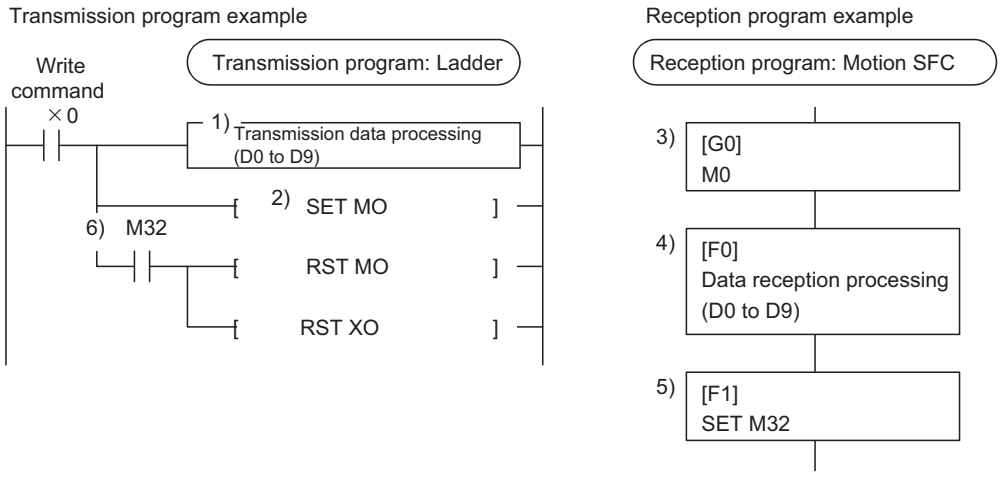
- Auto refresh between QCPU and Motion CPU

  Diagram 4.20 shows program examples for the Basic model QCPU and Motion CPU when Auto refresh settings in Multiple CPU settings are made as shown in Table 4.4.

<Parameter setting>

Table4.4 Parameter setting example for interlock program

Setting No.	CPU No.	CPU Shared Memory			CPU Side Device	
		Number of points	Start	End	Start	End
Setting 1	CPU No. 1	2	00C0	00C1	M0	M31
	CPU No. 2	2	0800	0801	M32	M63
Setting 2	CPU No. 1	10	00C2	00CB	D0	D9
	CPU No. 2	0	----	----	----	----



1) CPU No. 1 creates send data.
2) CPU No. 1 turns on the data setting completion bit.

<Auto refresh execution between multiple CPUs>

3) CPU No. 2 detects the completion of send data setting.
4) CPU No. 2 performs receive data processing.
5) CPU No. 2 turns on the completion of receive data processing.

<Auto refresh execution between multiple CPUs>

6) CPU No. 1 detects the completion of the receive data processing and turns off the data setting completion bit.

Diagram 4.20 Interlock program example

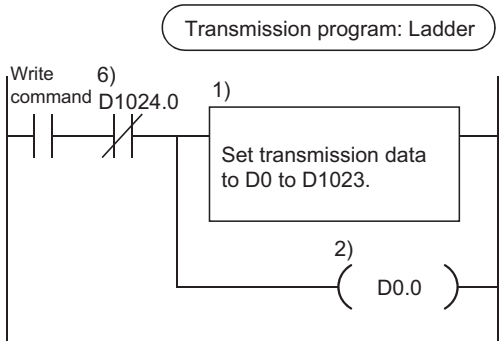
• Auto refresh between QCPUs
Diagram 4.21 shows program examples between the High Performance model QCPU when Auto refresh settings in Multiple CPU settings are made as Table 4.5.

<Parameter setting>

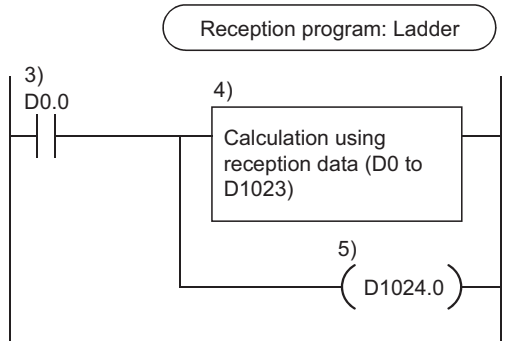
Table4.5 Parameter setting example for interlock program

Setting No.	CPU No.	CPU shared memory			Device at CPU	
		Number of points	Start	End	Start	End
Setting 1	CPU No. 1	1024	0000	03FF	D0	D1023
	CPU No. 2	1024	0000	03FF	D1024	D2047

Transmission program example



Reception program example



1) CPU No. 1 creates send data.
2) CPU No. 1 turns on the data setting completion bit.

<Auto refresh execution between multiple CPUs>
3) CPU No. 2 detects the completion of send data setting.
4) CPU No. 2 performs receive data processing.
5) CPU No. 2 turns on the completion of receive data processing.

<Auto refresh execution between multiple CPUs>
6) CPU No. 1 detects the completion of the receive data processing and turns off the data setting completion bit.

Diagram 4.21 Interlock program example

4.1.3 Communication by auto refresh using multiple CPU high speed transmission area

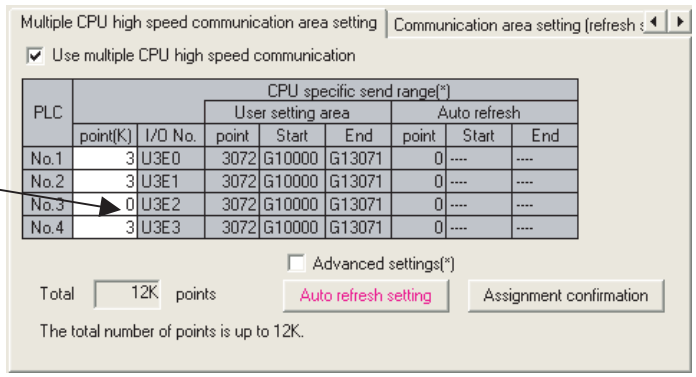
The following describes the communication by the auto refresh using the multiple CPU high speed transmission area in the Universal model QCPU.

The communication by the auto refresh using the multiple CPU high speed transmission area can be performed only when the following conditions are all met.

- The multiple CPU high speed main base unit (Q38DB or Q312DB) is used.
- The Universal model QCPU (Q03UDCPU, Q04UDHCPU, or Q06UDHCPU) is used as the CPU No.1.
- At least two modules (Universal model QCPU(s) (Q03UDCPU, Q04UDHCPU, and Q06UDHCPU) and/or Motion CPU(s) (Q172DCPU and Q173DCPU) are used.

The communication by the auto refresh using the multiple CPU high speed transmission area cannot be made with the CPU modules other than the Universal model QCPU (Q03UDCPU, Q04UDHCPU, and Q06UDHCPU) or the Motion CPU (Q172DCPU and Q173DCPU) that are mounted on the multiple CPU high speed main base unit.
When the module other than the Universal model QPCU (Q03UDCPU, Q04UDHCPU, and Q06UDHCPU) or the Motion CPU (Q172DCPU and Q173DCPU) is mounted on the multiple CPU high speed main base unit, set 0 to the number of points of the corresponding CPU in [each CPU send range].

Set 0 for the CPU modules other than the Universal model QCPU (Q03UDCPU, Q04UDHCPU, and Q06UDHCPU) or the Motion CPU (Q172DCPU and Q173DCPU).



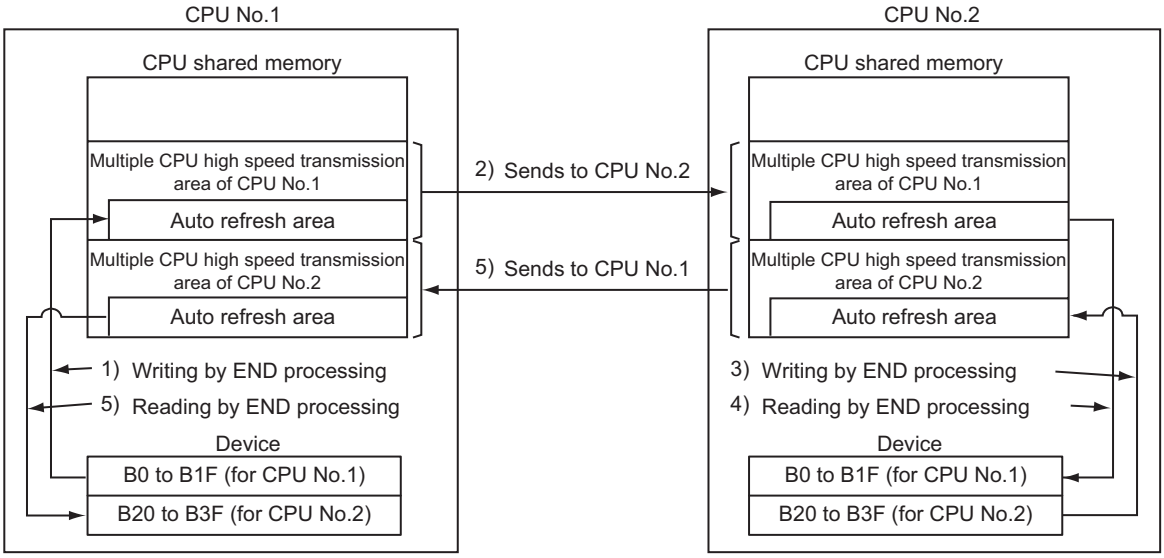
For "Communication by auto refresh using CPU shared memory", refer to Section 4.1.2.

(1) Communication using auto refresh

(a) Overview of auto refresh

The auto refresh is a communication method using the auto refresh area of the multiple CPU high speed transmission area in the CPU shared memory.
The data written to the auto refresh area of the multiple CPU high speed transmission area is sent to that of the other CPUs in a certain cycle (multiple CPU high speed transmission cycle).
Setting the PLC parameter "Multiple CPU settings" allows to automatically read/write data among all CPUs in the Multiple CPU system.
Since device data of other CPUs can be automatically read by the auto refresh function, the host CPU can also use them as those of host CPU.

Diagram 4.22 shows an outline of operations when CPU No.1 performs auto refresh of 32 points for B0 to B1F, and when CPU No.2 performs auto refresh of 32 points for B20 to B3F.



Procedure for the CPU No.2 to read device data of the CPU No.1

1) : Transfers data in B0 to B1F to auto refresh area of the host CPU at END processing of a CPU No.1.

2) : Sends data in multiple CPU high speed transmission area of CPU No.1 to CPU No.2.

3) : Transfers the received data to B0 to B1F at END processing of CPU No.2.

Procedure for the CPU No.1 to read device data of the CPU No.2

4) : Transfers data in B20 to B3F to auto refresh area of the host CPU at END processing of CPU No.2.

5) : Sends data in multiple CPU high speed transmission area of CPU No.2 to CPU No.1.

6) : Transfers the received data to B20 to B3F at END processing of CPU No.1.

Diagram 4.22 Outline of auto refresh operation

(b) Execution of auto refresh

Auto refresh is executed when the CPU module is in RUN, STOP or PAUSE status.

For auto refresh processing at error, refer to Section 4.1.5.

(c) Memory configuration of multiple CPU high speed transmission area

The following explains the memory configuration of the multiple CPU high speed transmission area of the CPU shared memory that is used in the multiple CPU high speed transmission function. (For the CPU shared memory, refer to Section 4.1.1.)

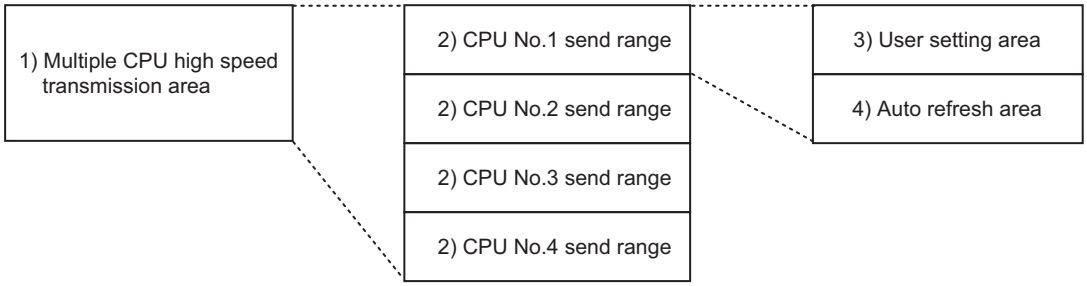


Diagram 4.5 Memory configuration of multiple CPU high speed transmission area

Table4.6 Description of multiple CPU high speed transmission area

No.	Name	Description	Size	
			Setting range	Setting unit
1)	Multiple CPU high speed transmission area	• Area for data transmission between each CPU modules in the Multiple CPU system. • The area up to 14k word is divided by each CPU module that constitutes the Multiple CPU system.	0 to 14k words	1k word
2)	CPU No. n send area n (n=1 to 4)	• Area to store the send data of the each CPU module. • Sends the data stored in the send area of the host CPU to the other CPUs. • Other CPU send area stores the data received from the other CPUs.	0 to 14k words	1k word
3)	User setting area	• Area for data communication with other CPUs using the multiple CPU area device. • Can be accessed by the user program using the multiple CPU area device.	0 to 14k words	2 words
4)	Auto refresh area	• Area for communicating device data with other CPUs by the communication using the auto refresh.	0 to 14k words	2 words

POINT

When the COM instruction is used in the sequence program, the auto refresh can be executed automatically at the execution of the COM instruction.
However, the scan time is prolonged due to the processing time for the auto refresh.
For details of the COM instruction, refer to the following manual.
☞ QCPU(Q mode)/QnACPU Programming Manual (Common Instructions)

(d) Settings required for auto refresh

To perform auto refresh, setting the number of points to be sent from each CPU module and a device for storing data (device for executing auto refresh) on Multiple CPU settings in PLC parameter is required.

(2) Multiple CPU high speed transmission area setting

To perform auto refresh in CPU shared memory, set the number of points to be sent from each CPU module (Send range for each PLC) and a device for storing data (Auto refresh settings) on Multiple CPU settings in PLC parameter.

(a) CPU specific send range setting

CPU specific send range setting sets the number of points of multiple CPU high speed transmission area that is allocated to the each CPU module which constitutes the Multiple CPU system.

CPU specific send range setting screen and the setting range are shown below.

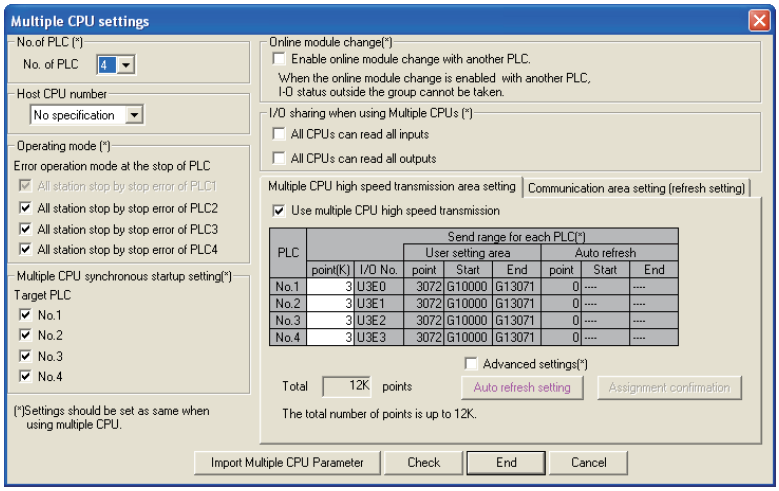


Diagram 4.6CPU specific send range setting screen

Table4.7 List of parameter setting/display item for CPU specific send renge setting

Item	Setting description	Setting/display value
CPU specific send range	Sets the number of points of data that each CPU module sends.*1	Setting range: 0 to 14.0k points*4 Setting unit: 1.0k point
User setting area	Used when communicating with the other CPU using the program. The value where the "number of points set in the auto refresh" is subtracted from the "CPU specific send range setting" is displayed.	Display range: 0 to 14335 points
Auto refresh	Used when communicating with the other CPU using the auto refresh. Number of points that is set by the "auto refresh setting" is displayed.	Display range: 0 to 14335 points

* 1: The following number of points is set by the default.

Number of CPUs	Default value of CPU specific send range			
	CPU No.1	CPU No.2	CPU No.3	CPU No.4
Two CPUs	7k points	7k points	----	----
Three CPUs	7k points	3k points	3k points	----
Four CPUs	3k points	3k points	3k points	3k points

* 2: Sets the total of all CPUs to be the following points or lower.
- When constituted with two CPUs: 14k points
- When constituted with three CPUs: 13k points
- When constituted with four CPUs: 12k points

POINT

Selecting "Advanced settings" enables to change the number of points in Restricted system area used for dedicated instructions to 2 k points.
Changing the number of points in system area to 2 k enables to increase the number of dedicated instructions can be executed concurrently in a scan.
The following shows the setting screen and setting range of the case where "Advanced settings" is selected.

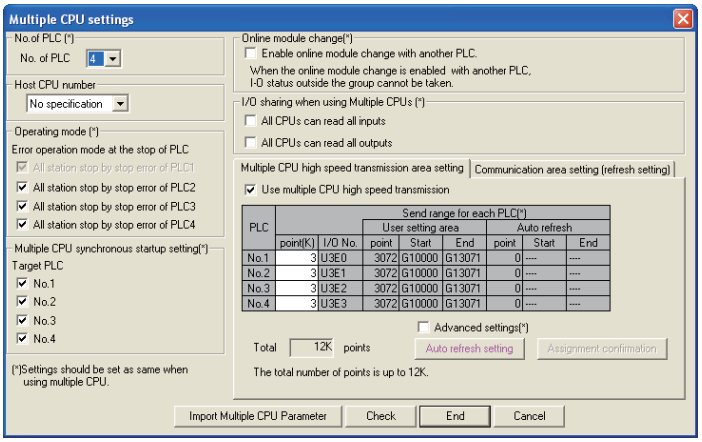


Diagram 4.7 CPU specific send range setting screen

Table4.8 List of parameter setting/display item for CPU specific send range setting

Item	Setting description	Setting/display value
CPU specific send range	Sets the number of points of data that each CPU module sends.	Setting range: 0 to 14k points*1 Setting unit: 1k point
Restricted system area	The system area is used for "dedicated instructions"*3 Set the number of points for a system area to be assigned for each CPU module.	Setting range: 1k point to 2k point
Total	Displays the total of number of points of the host CPU send area and the restricted system area that are allocated to the each CPU module.	Setting range: 1 to 16k points*2 Setting unit: 1k point*7

* 1: Sets the total of all CPUs to be the following point or lower.
When constituted with two CPUs: 14k points
When constituted with three CPUs: 13k points
When constituted with four CPUs: 12k points
* 2: Sets the total of all CPUs to be 16.0k points or lower.
* 3: For "dedicated instructions", refer to the manual of the Motion CPU.

(b) Auto refresh setting

Auto refresh setting is a setting to use the auto refresh function.
The 32 ranges can be set for each CPU modules.
Auto refresh setting screen and the setting range are shown below.

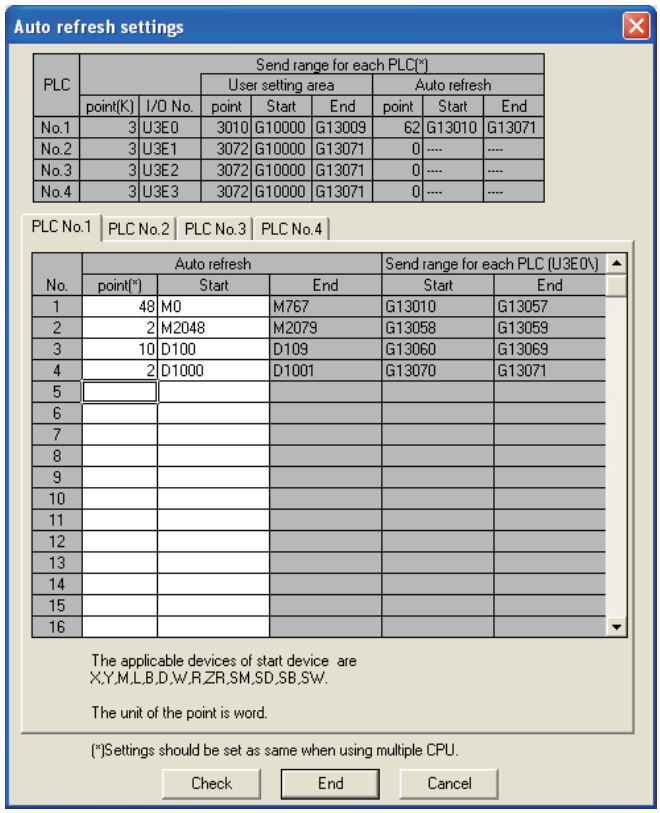


Diagram 4.8 Auto refresh setting screen

Table4.9 List of setting item for the refresh setting

Item	Setting description	Setting range
Number of points	Specifies the number of points for data communication in word unit.	• Setting range: 2 to 14336 points*1 • Setting unit: 2 points*2
Start	Specifies the device which performs the data communication (auto refresh). Specifies the device sent by the host CPU when the CPU specific send range setting is the host CPU, and specifies the device received by the host CPU when the CPU specific send range setting is the other CPU.	• Device available for send range*3 : X, Y, M, L, B, D, W, R, ZR, SM, SD, SB, SW • Device available for receive range*3 : X, Y, M, L, B, D, W, R, ZR Sets "blank" when auto refresh is not executed.

* 1: Setting which exceeds the number of points of the host CPU send area allocated to the each CPU module (CPU specific send range) cannot be set.
* 2: Bit device can be specified in units of 32 points (2 words) only.
* 3: Device number is No.1 to No.32, which cannot be duplicated.

(3) Auto refresh setting and data flow

The following explains the data flow among CPU modules when a multiple CPU system is configured among three CPU modules and auto refresh is set for two ranges.

(a) Setting examples of auto refresh to each CPU module

Diagram 4.27 shows the setting examples of auto refresh to explain the data flow by auto refresh.

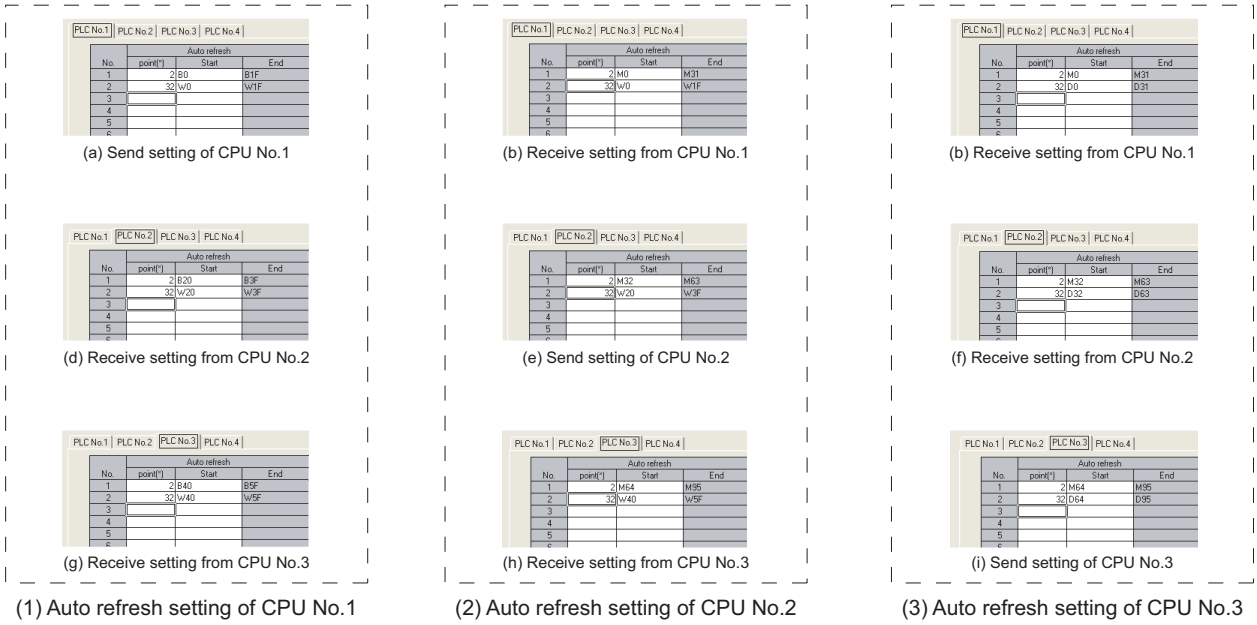


Diagram 4.27 Setting examples of auto refresh

(b) Data flow among CPU modules

The following explains the data flow among CPU modules by the auto refresh set as (a).

1) Flow of sending data from CPU No.1 to other CPUs

<Parameter setting>

Diagram 4.28 shows the settings related to sending and receiving CPU No.1 data ((a) to (c) in Diagram 4.27) in the setting example of auto refresh in Diagram 4.27.

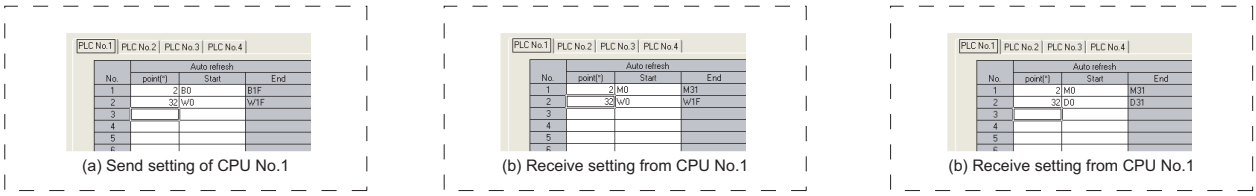
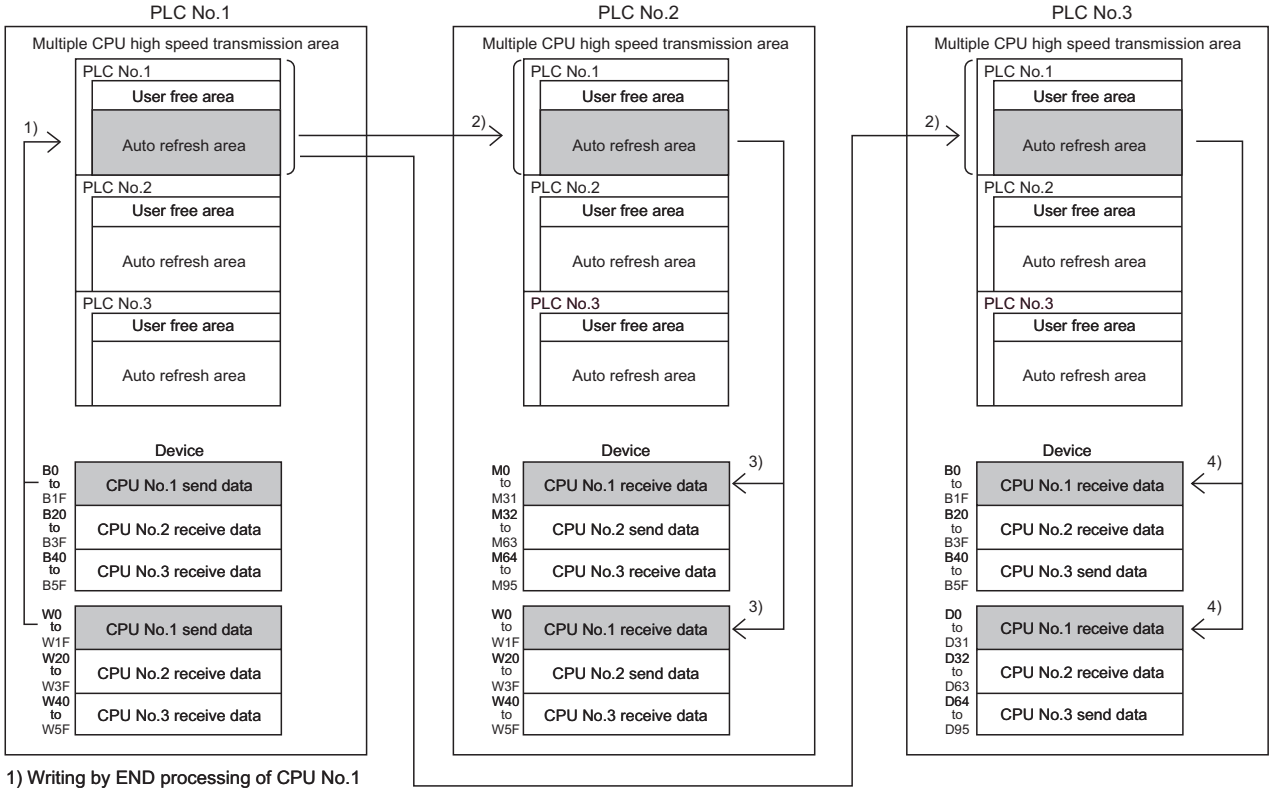


Diagram 4.28 Auto refresh setting related to sending and receiving CPU No.1 data

<Flow of sending data from CPU No.1 to other CPUs>

- CPU No.1 writes device data set in Auto refresh (CPU No.1 send data) to the auto refresh area in CPU No.1 at END processing.
- CPU No.1 sends data in auto refresh area of CPU No.1 to CPU No.2 and CPU No.3 in multiple CPU high speed transmission cycle.
- CPU No.2 and No.3 read the received data from CPU No.1 to a device set in Auto refresh (CPU No.1 receive data) at END processing.



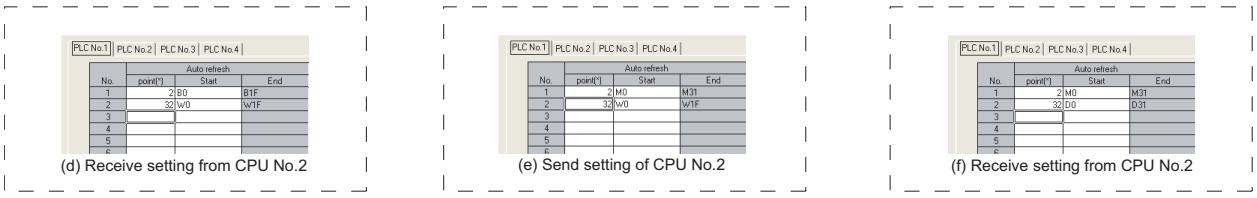
1) Writing by END processing of CPU No.1
2) Sending data from CPU No.1 to CPU No.2 and CPU No.3
3) Reading by END processing of CPU No.2
4) Reading by END processing of CPU No.3

Diagram 4.29 Flow of sending data from CPU No.1 to other CPUs

2) Flow of sending data from CPU No.2 to other CPUs

<Parameter setting>

Diagram 4.30 shows the settings related to sending and receiving CPU No.2 data ((d) to (f) in Diagram 4.27) in the setting example of auto refresh in Diagram 4.27.

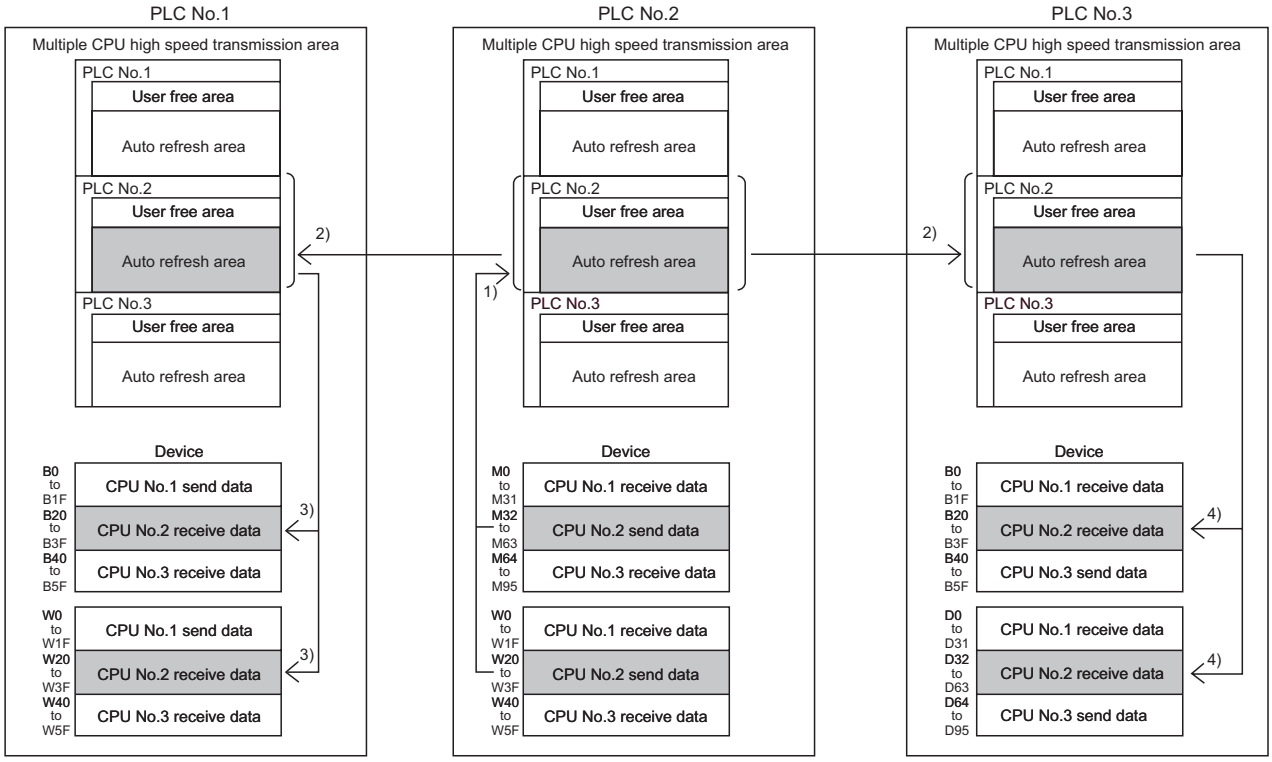


(1) Auto refresh setting of CPU No.1 (2) Auto refresh setting of CPU No.2 (3) Auto refresh setting of CPU No.3

Diagram 4.30 Auto refresh setting related to sending and receiving CPU No.2 data

<Flow of sending data from CPU No.2 to other CPUs>

- CPU No.2 writes device data set in Auto refresh (CPU No.2 send data) to the auto refresh area in CPU No.2 at END processing.
- CPU No.2 sends data in auto refresh area of CPU No.2 to CPU No.1 and CPU No.3 in multiple CPU high speed transmission cycle.
- CPU No.1 and No.3 read the received data from CPU No.2 to a device set in Auto refresh (CPU No.2 receive data) at END processing.



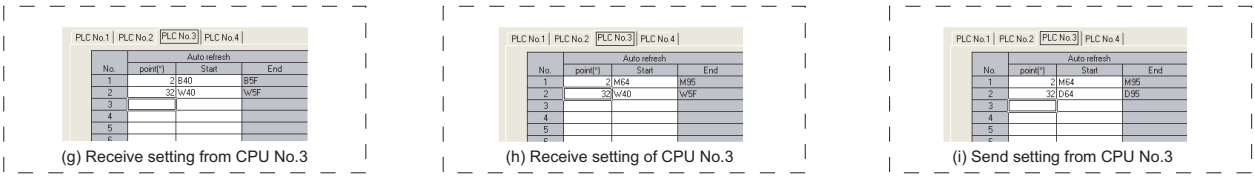
1) Writing by END processing of CPU No.2
2) Sending data from CPU No.2 to CPU No.1 and CPU No.3
3) Reading by END processing of CPU No.1
4) Reading by END processing of CPU No.3

Diagram 4.31 Flow of sending data from CPU No.2 to other CPUs

3) Flow of sending data from CPU No.3 to other CPUs

<Parameter setting>

Diagram 4.32 shows the settings related to sending and receiving CPU No.3 data ((g) to (i) in Diagram 4.27) in the setting example of auto refresh in Diagram 4.27.



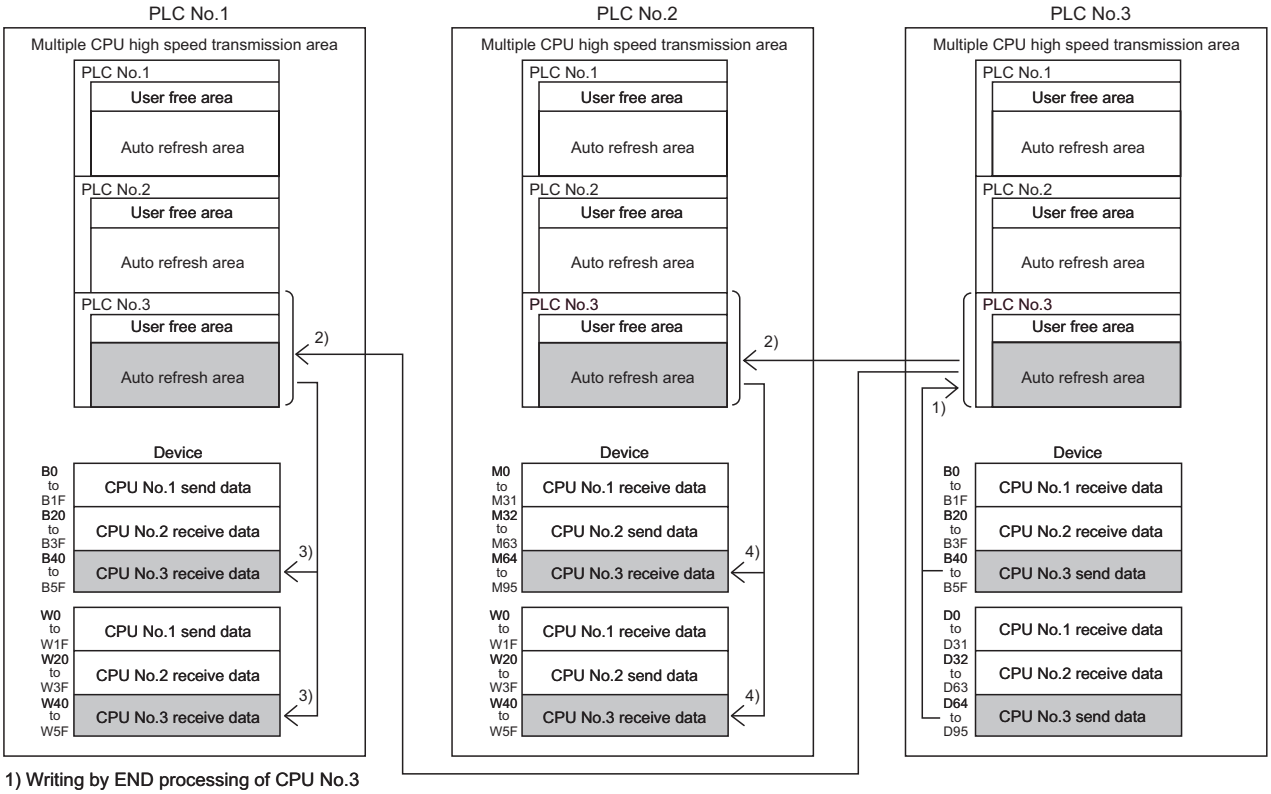
(g) Receive setting from CPU No.3 (h) Receive setting of CPU No.3 (i) Send setting from CPU No.3

(1) Auto refresh setting of CPU No.1 (2) Auto refresh setting of CPU No.2 (3) Auto refresh setting of CPU No.3

Diagram 4.32 Auto refresh setting related to sending and receiving CPU No.3 data

<Flow of sending data from CPU No.3 to other CPUs>

- CPU No.3 writes device data set in Auto refresh (CPU No.3 send data) to the auto refresh area in CPU No.3 at END processing.
- CPU No.3 sends data in auto refresh area of CPU No.3 to CPU No.1 and CPU No.2 in multiple CPU high speed transmission cycle.
- CPU No.1 and No.2 read the received data from CPU No.3 to a device set in Auto refresh (CPU No.3 receive data) at END processing.



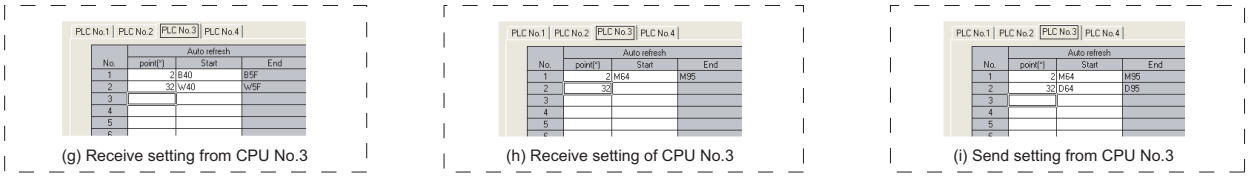
1) Writing by END processing of CPU No.3
2) Sending data from CPU No.3 to CPU No.1 and CPU No.2
3) Reading by END processing of CPU No.1
4) Reading by END processing of CPU No.2

Diagram 4.33 Flow of sending data from CPU No.3 to other CPUs

POINT

If Start and End fields in Auto refresh are left blank, auto refresh is not performed.
The example for setting blank to the auto refresh setting .of the CPU No.2 in <Flow of sending data from CPU No.3 to other CPUs> explained in the previous page 3) is shown below.
In the auto refresh setting of CPU No.2 in Diagram 4.32, if the Start (W40) and End (W5F) fields of the Auto refresh are left blank, auto refresh is not performed to W40 to W5F in CPU No.2.

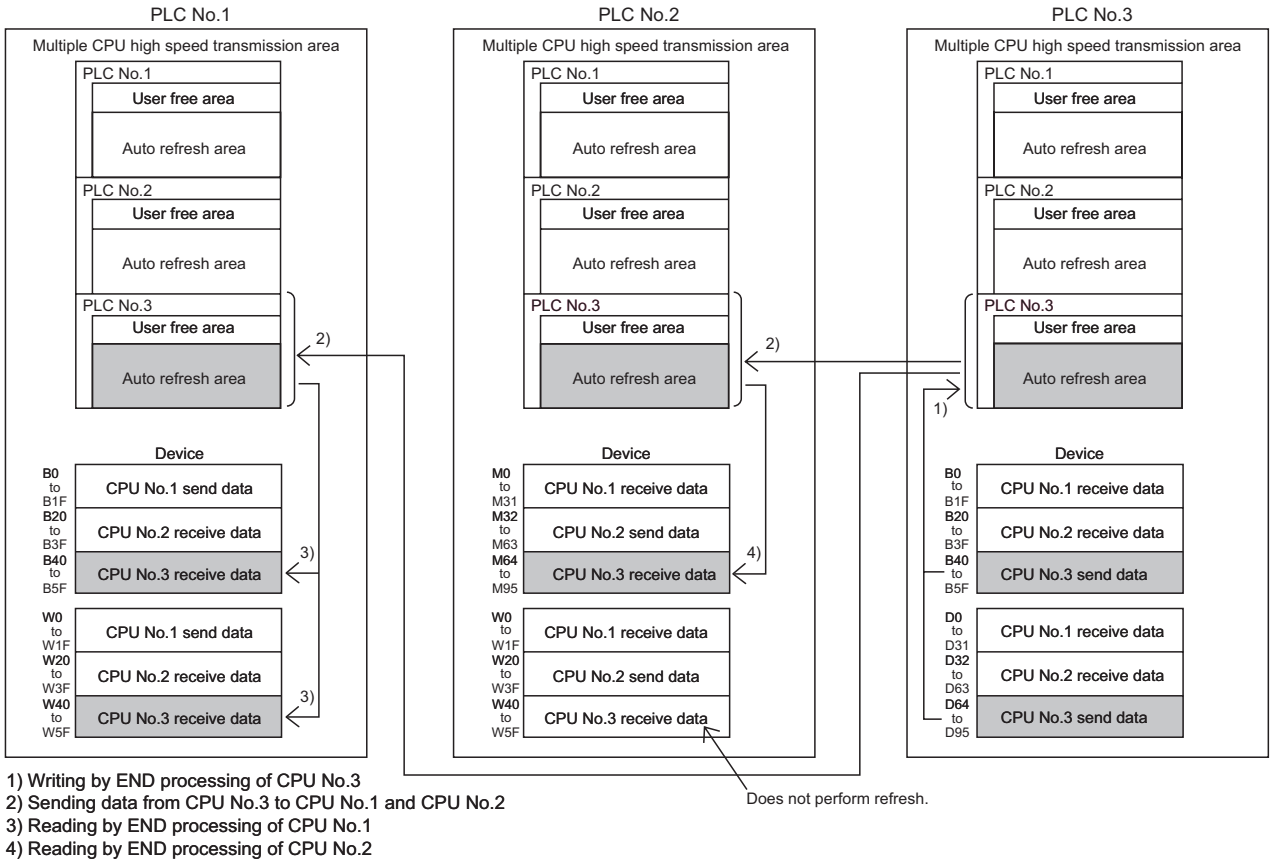
<Parameter setting>



(1) Auto refresh setting of CPU No.1 (2) Auto refresh setting of CPU No.2 (3) Auto refresh setting of CPU No.3

Diagram 4.34 Auto refresh setting related to sending and receiving CPU No.3 data (Leaving the second row of PLC No.2 blank)

<Flow of sending data from CPU No.3 to other CPUs>
For flow of sending data from CPU No. 3, refer to 3) Flow of sending data from CPU No.3 to other CPUs on the previous page.



1) Writing by END processing of CPU No.3
2) Sending data from CPU No.3 to CPU No.1 and CPU No.2
3) Reading by END processing of CPU No.1
4) Reading by END processing of CPU No.2

Diagram 4.35 Flow of sending data from CPU No.3 to other CPUs

(4) Precautions

(a) Local device setting

Device ranges set for the use of the auto refresh cannot be set to local devices. If set, the refresh data will not be updated.

(b) Setting for using the same file name as the program in the file register

Do not set devices for the use of the auto refresh in the file register for each program.
If set, auto refresh will be performed on the file register that corresponds to the last scan execution type program executed.

(c) Transmission delay time

Data transmission delay time due to auto refresh is from 0.09 ms to (1.80 + (Sending side scan time + Receiving side scan time $\times$2)) ms.

(d) Assurance of data sent between CPUs

Due to the timing of data send from the host CPU and auto refresh in any of other CPUs, old data and new data may be mixed (data separation) in each CPU.
The following shows the methods for avoiding data separation at communications by auto refresh.

1) Data consistency for 32 bit data

Transfer data with auto refresh method in units of 32 bits. Since auto refresh is set in units of 32 bits, 32-bit data does not separate.

2) Data consistency for data exceeding 32 bits

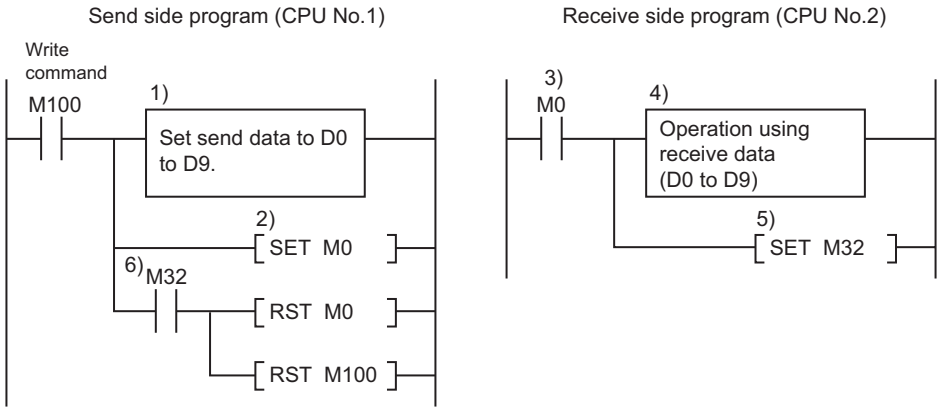
In auto refresh method, data are read in descending order of the setting number in auto refresh setting parameter.
Transfer data separation can be avoided by using the transfer number lower than the transfer data as an interlock device.
Diagram 4.36 shows a program example for interlocking between CPU No.1 and CPU No.2.

<Parameter setting>

Table4.10 Example for parameter setting for interlock program

CPU No.1 auto refresh setting							Direction	CPU No.2 auto refresh setting						
CPU No.	Transfer No.	Data communication range for each CPU			Device setting for data communication			CPU No.	Transfer No.	CPU specific send range			Device setting for data communication	
		Number of points	Start	End	Start	End				Number of points	Start	End	Start	End
CPU No.1	Transfer 1	2	0	1	M0	M31	→	CPU No.1	Transfer 1	2	0	1	M0	M31
	Transfer 2	10	2	11	D0	D9			Transfer 2	10	2	11	D100	D109
CPU No.2	Transfer 1	2	0	1	M32	M63	←	CPU No.2	Transfer 1	2	0	1	M32	M63

In the above parameter settings, use M0 as an interlock device for CPU No.1 (data setting completion bit) and M32 as an interlock device for CPU No.2 (receive data processing completion bit).



1) CPU No.1 stores the send data to D0 to D9.

2) CPU No.1 turns on the data setting completion bit (MO).

Writes the above data to the auto refresh area of the CPU No.1 send area at the END processing of the CPU No.1.
Sends the data in the auto refresh area of the CPU No.1 send area to the CPU No.2.
Reads the received data to the specified device at END processing of CPU No.2.

3) CPU No.2 detects the send data setting completion.

4) CPU No.2 performs the receive data processing.

5) CPU No.2 turns on the receive data processing completion.

Writes the above data (5) to the auto refresh area of the CPU No.2 send area at the END processing of the CPU No.2.
Sends the data in the multiple CPU high speed transmission area of the CPU No.2 to the CPU No.1.
Reads the received data to the specified device at END processing of CPU No.1.

6) CPU No.1 detects the receive data processing completion and turns off the data setting completion bit.

Diagram 4.36 Example for interlock program

4.1.4 Communication using CPU shared memory by program

This section explains communications with programs using CPU shared memory in a multiple CPU system.
Use the following areas in a CPU shared memory for the communications with programs using CPU shared memory.

- User setting area
- User setting area in multiple CPU high speed transmission area

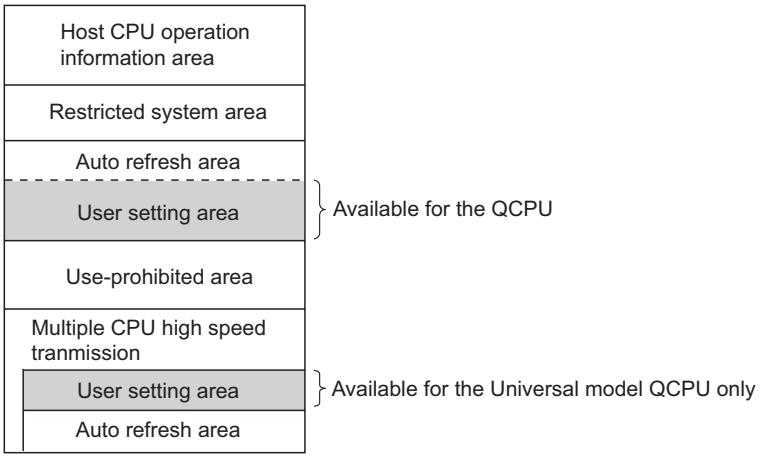


Diagram 4.37 Example for interlock program

POINT

The user setting area of the multiple CPU high speed transmission area is available for the following CPU modules only.

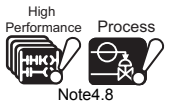
- Universal model QCPU (except Q02UCPU)
- Motion CPU (Q172DCPU, Q173DCPU)

(1) Communication made by program

(a) Instructions used for writing to/reading from the CPU shared memory

The QCPU in a multiple CPU system enables to communicate each CPU module using user free areas in CPU shared memory and multiple CPU high speed transmission area with the write and read instructions.
The table 4.11 shows the write/read instruction.

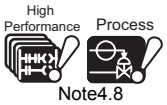
Table4.11 List of write and read instructions



	Description
Write instruction*3	• Instruction using the multiple CPU area device (U3En\G□)*1 • TO instruction Note4.8 • S.TO instruction *2
Read instruction*3	• Instruction using the multiple CPU area device (U3En\G□)*1 • FROM instruction *2

* 1: When accessing multiple CPU high speed transmission area, the processing speed is faster than when using any of the TO, DTO, FROM or DFRO instructions.
* 2: Using the S.TO instruction, data cannot be written to user setting area in multiple CPU high speed transmission area.
* 3:For the TO/DTO/S.TO instruction (write instruction) and the FROM/DFRO instruction (read instruction), refer to the following manual.

☞ QCPU(Q mode)/QnACPU Programming Manual(Common Instructions)

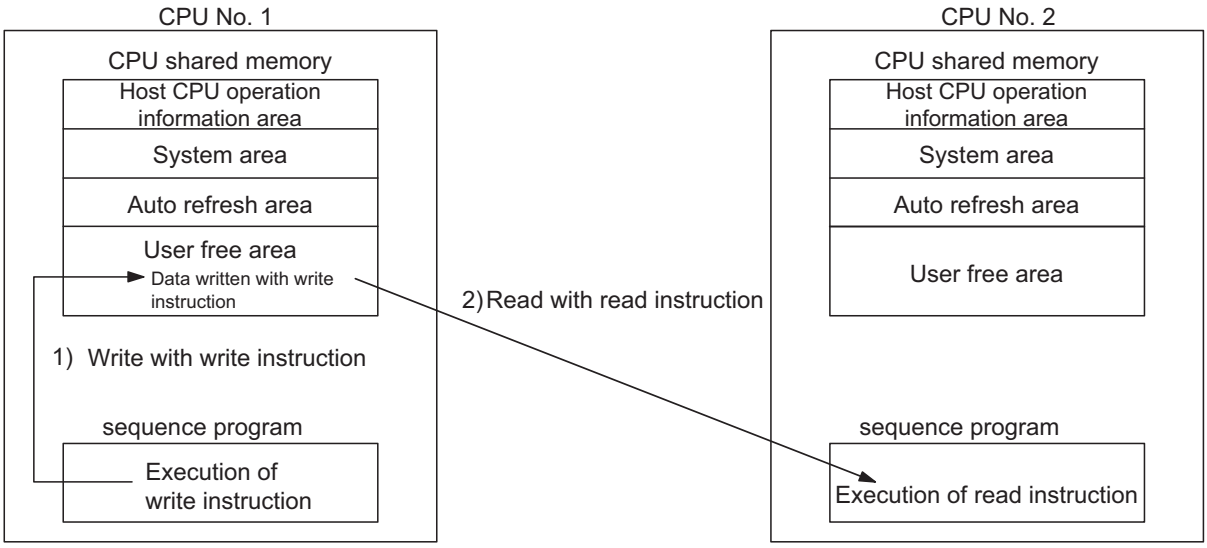


For the High Performance model QCPU or the Process CPU, write to the CPU shared memory with TO instruction is not allowed.

(b) Outline of the communication by the program

1) Using user setting area

The data written to the CPU shared memory of the host CPU with a write instruction can be read by another CPU using a read instruction.
Unlike the auto refresh of the CPU shared memory, it is possible to read up-to-date data directly when this instruction is executed.
An outline of a process where data written in the CPU shared memory of CPU No.1 with an write instruction is read by CPU No.2 using an read instruction is shown in Diagram 4.22.



CPU No.1 processing

1) Data are written into the user setting area of CPU No.1 with a write instruction.

CPU No.2 processing

2) A read instruction is used to read data from the user setting area of CPU No.1 to the specified device.

Diagram 4.22 Outline of communication by program

For the write/read instruction, refer to Section 4.1.4 (1).

POINT

For the Motion CPU, the write/read instructions are not usable.
For the accessing method from the Motion CPU and PC CPU module to the CPU shared memory, refer to each CPU module manual.

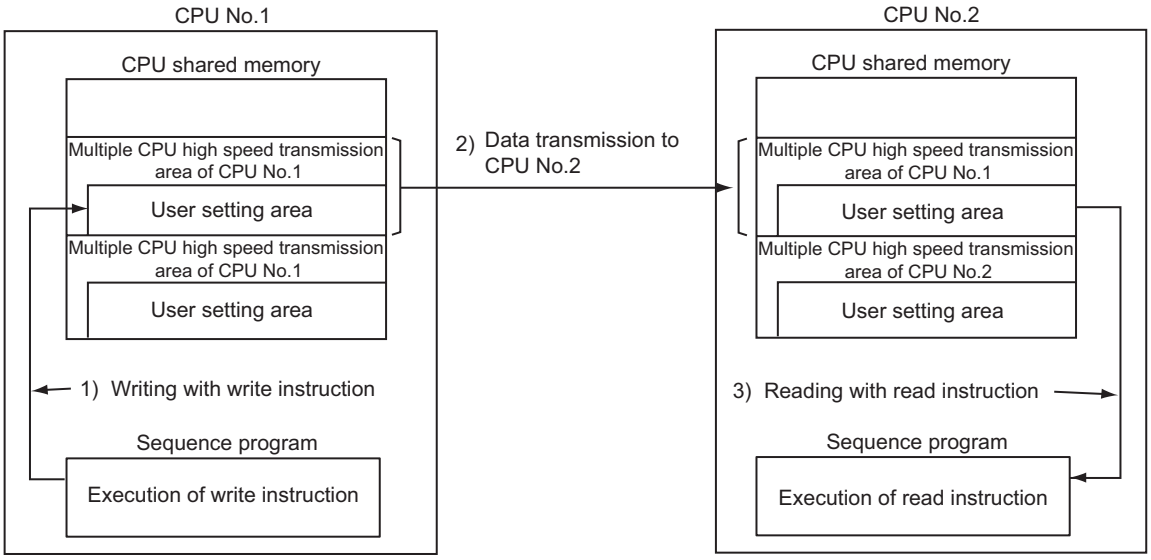
2) Using user setting aera in multiple CPU high speed transmission area

The data written to the multiple CPU high speed transmission area of the CPU shared memory of the host CPU by the write instruction is sent to the other CPU in a certain cycle.

The other CPU reads the receive data from the multiple CPU high speed transmission area of the CPU shared memory by the read instruction.

The other CPU can read the data of the multiple CPU high speed transmission area of the CPU shared memory at the execution of the instruction, which is different from the auto refresh of the CPU shared memory.

The figure 4.10 shows the outline of operation where the data written to the CPU shared memory of the CPU No.1 using the write instruction is read by the CPU No.2 using the read instruction.



Procedure for the CPU No.2 to read device data of the CPU No.1

1) Writes data in the user free area of the multiple CPU high speed transmission area of the CPU No.1 by the write instruction.
2) Sends the data in the multiple CPU high speed transmission area of the CPU No.1 to that of the CPU No.2.
3) Reads the data in the user setting area of the CPU No. 1 to the specified device from the multiple CPU high speed transmission area of the host CPU by the read instruction.

Diagram 4.10 Outline of communication by the program

For the write/read instruction, refer to Section 4.1.4 (1).

POINT

(1) For the Motion CPU, the write/read instructions cannot be used.
For the method to access from the Motion CPU to the multiple CPU high speed transmission area of the CPU shared memory, refer to the manual for the Motion CPU.

(2) The delay time of data transfer with programs using user setting area in multiple CPU high speed transmission area is from 0.09 ms to 1.80 ms.

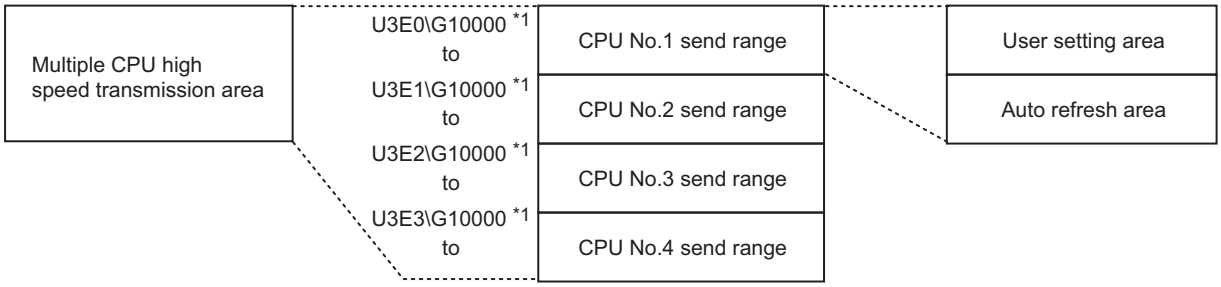
(c) Memory configuration of multiple CPU high speed transmission area

1) Addresses of user setting area

The addresses of user setting area depend on the CPU module.
For user setting area addresses, refer to Section 4.1.1.

2) Addresses of multiple CPU high speed transmission area

The following explains the memory configuration of the multiple CPU high speed transmission area that is used in the multiple CPU high speed transmission function. (For the CPU shared memory, refer to Section 4.1.1.)



* 1:Indicates addresses when user setting area for each CPU is specified using multiple CPU devices.

Diagram 4.11 Memory configuration of multiple CPU high speed transmission area

For the each area of the multiple CPU high speed transmission area, refer to Section 4.1.3.

High Performance Process Basic Note4.9

Universal UD Note4.9

(2) Parameter setting*Note4.9*

When performing the auto refresh of the multiple CPU high speed transmission area, the number of points to be sent by each CPU module is set in the PLC parameter "Multiple CPU settings."
For the setting description of the parameter, refer to Section 4.1.3.

High Performance Process Basic Note4.9

Universal UD Note4.9

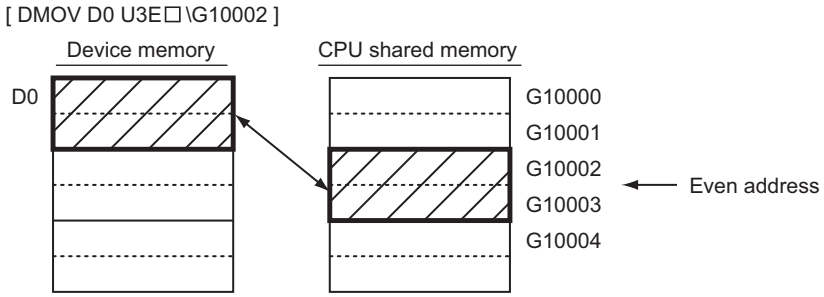
For the High Performance model QCPU, Process CPU, Basic model QCPU, Q02UCPU, parameter setting can be ignored since the user setting area of the multiple CPU high speed transmission area is not available.

(3) Assurance of data sent between CPUs

The old data and the new data may be mixed in each CPU due to the timing of receiving data from the other CPU and reading in the host CPU.
The following shows the method to realize the data consistency of the user data for the data transmission in the multiple CPU high speed transmission function.

(a) Data consistency for 32 bit data

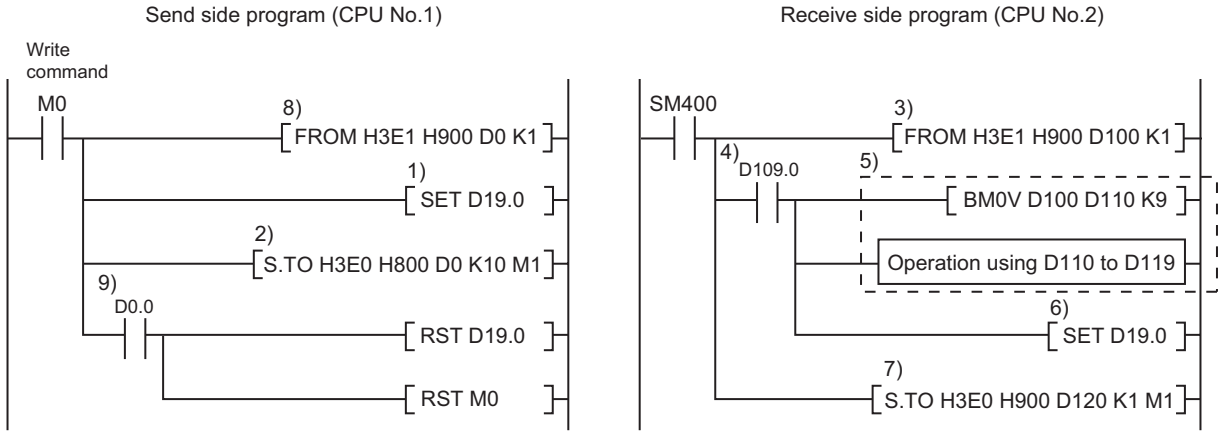
Accessing to the user setting area of the multiple CPU high speed transmission area with placing the address of even number in front (for example, address 10002) can realize the data consistency for 32 bit data.



(b) Data consistency for data exceeding 32 bits

1) Using user setting area

Programs are read from the start of user setting area.
Creating an interlock device at the end of data for communications, the data separation can be prevented.
An example for the program which interlocks CPU No.1 and CPU No.2 is shown in Figure 4.41



1) Turns ON send data set completion flag (D19.0).
2) Writes send data (D10 to D19) to user setting area.
3) The CPU No. 2 reads the send data of the CPU No.1.
4) Detects that send data set completion flag of the CPU No.1 turns ON.
5) The CPU No.2 processes the receive data.
6) The CPU No.2 turns ON the processing completion flag of the receive data (D120.0).
7) The CPU No. 2 writes the processing completion of the receive data to user setting area.
8) Reads read completion flag of the CPU No.2 to D0.
9) The CPU No.1 detects that the receive data processing completion flag turns ON and turns OFF send data set completion flag.

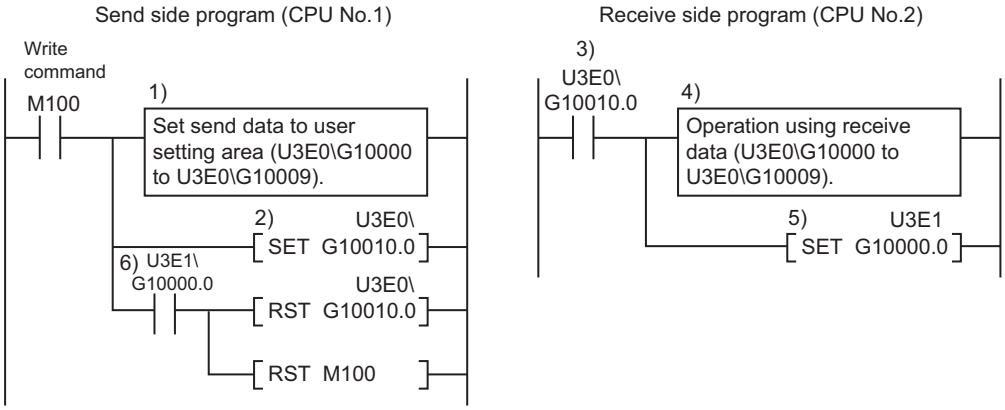
Diagram 4.41 Example for interlock program

2) Using multiple CPU high speed transmission area

In the direct access mode, the data is transferred in order starting from the one which was written to the user setting area first.

Using the device which is written after the data transfer regardless of kinds of device or addresses can realize the data consistency of the transferred data.

Example for program executing interlock in CPUs No.1 and No.2 is shown in Figure 4.14.



(1) The CPU No.1 writes the send data (D0 to D9) to the user setting area.

(2) The CPU No.1 writes "ON" of the data setting completion bit to the user setting area.

<The data in the multiple CPU high speed transmission area of the CPU No.1 is sent to the CPU No.2.>

(3) The CPU No.2 detects the send data setting completion.

(4) The CPU No.2 performs the receive data processing.

(5) The CPU No.2 writes "ON" of the receive data processing completion to the user setting area.

<The data in the multiple CPU high speed transmission area of the CPU No.2 is sent to the CPU No.1.>

(6) CPU No.1 detects "ON" of the receive data processing completion and turns off the data setting completion bit.

Diagram 4.14 Example for interlock program

(4) Precautions

(a) First I/O numbers of CPU modules

The following values are set for the CPU module's first I/O number in the write/read instructions.

Basic Note4.10

Table4.12 First I/O numbers of CPU modules

CPU No.	CPU No.1	CPU No.2	CPU No.3	CPU No.4 *Note4.10*
Value set in the first I/O number	$3E0_H$	$3E1_H$	$3E2_H$	$3E3_H$

High Performance Process Note4.11

(b) Writing to CPU shared memory

Do not write data to the following areas in the CPU shared memory. *Note4.11*
(☞ Section 4.1.1)

- Restricted system area
- Auto refresh area

(c) Access to module in reset status

No error will occur even if the CPU accessed with a write instruction is in reset status.

Universal UD Note4.12

However, access execution flag (SM390) *Note4.12* will remain OFF after the instruction execution has been completed.

(d) Simultaneous access to CPU module

Establish an interlock to prevent simultaneous access during interactive data communication with write/read instructions.
Old data and new data may be mixed together if simultaneous access is carried out.(☞ Section 4.1.2)

Basic Note4.10

Since the number of CPU modules that can be mounted is up to 3 when using the basic model QCPU, there is no CPU No.4.

High Performance Process Note4.11

For the High Performance model QCPU or the Process CPU, reading data from "Restricted system area" and "Auto refresh area" is not also allowed.

Universal UD Note4.12

An access executing flag (SM390) is unavailable for the Universal model QCPU.

(e) Data writing to other CPU's shared memory

Data cannot be written to the CPU shared memory of other CPU with a write instruction.

Writing data to the CPU shared memory of other CPU No. with TO, S.TO instructions or those using the multiple CPU area device (U3En\G□) may result in "SP. UNIT ERROR (error code: 2115)".

(f) Data writing to host CPU's shared memory

1) Basic model QCPU

Data can be written to the host CPU's shared memory with a write instruction.

2) High Performance model QCPU or Process CPU

Data can be written to the host CPU's shared memory with the S.TO instruction, not with the instruction using the multiple CPU area device (U3En\G□).

Writing data to the host CPU's shared memory with the instruction using the multiple CPU area device (U3En\G□) results in "SP.UNIT ERROR (Error code: 2114)".

3) Universal model QCPU

Data can be written to the host CPU's shared memory with a write instruction.

(g) Data reading from CPU shared memory

1) Basic model QCPU

Data can be read from the host CPU's shared memory with a read instruction.

2) High Performance model QCPU or Process CPU

Data cannot be read from the host CPU's shared memory with a read instruction.

Doing so results in "SP.UNIT ERROR (Error code: 2114)".

3) Universal model QCPU

Data can be read from the host CPU's shared memory with a read instruction.

(h) Access to CPU that is not actually installed

Access to the CPU that is not actually installed with an instruction using the multiple CPU area device (U3En\G□) is not allowed.

Doing so leads to "SP.UNIT ERROR (Error code: 2110)".

4.1.5 Communications between CPU modules when the error occurs

(1) Operation when the error occurs to the receive data

When the CPU module receives the improper data at the data communication between the CPU modules due to noise or failure, it cancels the receive data.
When the receive data is canceled, the data which was received before this one remains without change.
When the normal data is received in the next time, it will be updated to the receive data.

(2) Data transmission operation when the error occurs

Table 4.17 shows the auto refresh and the data communication between CPU modules when the host CPU detects the self-diagnostics error.

Table4.13 Data communication between CPU modules when the self-diagnostics error occurs

Error definition		Auto refresh*1	Data communication between CPU modules*2
Slight error		○	○
Moderate error	Factors other than below	○	○
	Errors on multiple CPU high speed transmission function parameter (including the consistency check error)	× *4	× *4
Severe error		×	× *3

○:Transfer, ×:Does not transfer

* 1: Shows the data transfer between the internal user device and the multiple CPU high speed transmission area of the host CPU.
* 2: Shows the data communication between the multiple CPU high speed transmission area of the host CPU and the multiple CPU high speed transmission area of the other CPU.
* 3: When the error occurs during the normal operation, transmission of the normal data before the error occurs is continued.
* 4: Continues sending/receiving data between the auto refresh area 0 and CPU module if consistency check error occurs due to PLC parameter change during normal operation.

POINT

The communication between CPU modules when the error occurs can be executed if the following CPU modules are used.

- Universal model QCPU (except Q02UCPU)
- Motion CPU (Q172DCPU, Q173DCPU)

4.2 Communications with instructions dedicated to Motion CPU

4.2.1 Control instruction from QCPU to Motion CPU

Control instructions can be issued from the QCPU to Motion CPU with the instructions dedicated to Motion CPU as listed in Table4.14.

(Control instructions from a Motion CPU to other Motion CPU is not allowed.)

Table4.14 List of instructions dedicated to Motion CPU

Instruction name	Description	CPU module		
		Basic model QCPU/ High Performance model QCPU/ Process CPU	Universal model QCPU	
			Q02UCPU	Q03UDCPU Q04UDHCPU 06UDHCPU
S.SFCS SP.SFCS	Requests startup of the motion SFC program.	○	○	×
D.SFCS DP.SFCS		×	×	○
S.SVST*1 SP.SVST*1	Requests the start of the servo program.	○	○	×
D.SVST DP.SVST		×	×	○
S.CHGV*1 SP.CHGV*1	Changes the speed of the axes during positioning and JOG operations.	○	○	×
D.CHGV DP.CHGV		×	×	○
S.CHGT*1 SP.CHGT*1	Changes the torque control value during operation and suspension when in the real mode.	○	○	×
D.CHGT DP.CHGT		×	×	○
S.CHGA*1 SP.CHGA*1	Changes the current values of the halted axes, the synchronized encoder, and the cam axes.	○	○	×
D.CHGA DP.CHGA		×	×	○

○: Available, ×: Not Available

* 1: The following version restrictions apply to the Motion CPU.
Q172CPU : Version N or later
Q173CPU : Version M or later
Q172CPUN, Q173CPUN : No version restriction
Q17H2CPU, Q173HCPU : No version restriction

(Example) When using the S.SFCS instruction
It is possible to start up the Motion CPU's motion SFC from the QCPU.

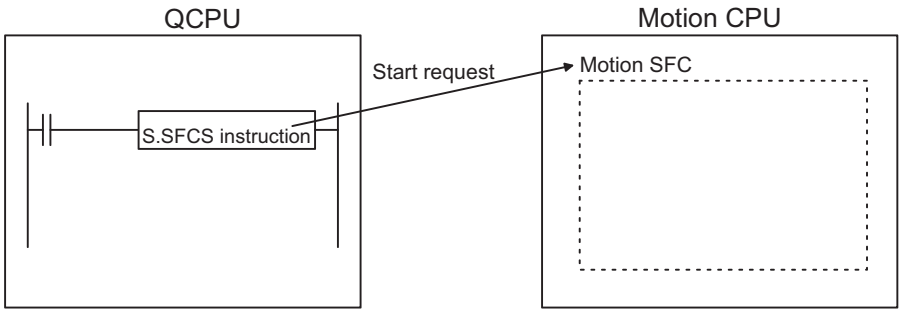


Diagram 4.23 Operation of S.SFCS instruction

POINT

One QCPU can concurrently issue up to 32 instructions of "Instructions dedicated to Motion CPU" and "Instructions dedicated to communication between multiple CPUs (except for S(P).GINT)".
Note that multiple instructions are executed in order starting from the first instruction.
When 33 or more incomplete instructions are identified, an "OPERATION ERROR (error code: 4107)" occurs.

Remark

Refer to the Motion CPU manual for details on the use of the insructions dedicated to Motion CPU.

4.3 Communication between multiple CPUs with dedicated instructions

4.3.1 Write/read of device data from QCPU to Motion CPU

Device data can be read or written from the QCPU to the Motion CPU with the instructions dedicated to communication between multiple CPUs listed in Table4.15.
(Read/write from a Motion CPU to other CPU module including the Motion CPU is not allowed.)

Table4.15 List of instructions dedicated to communication between multiple CPUs available for Motion CPU

Instruction name	Description	CPU module		
		Basic model QCPU/ High Performance model QCPU/ Process CPU	Universal model QCPU	
			Q02UCPU	Q03UDCPU Q04UDHCPU 06UDHCPU
S.DDWR SP.DDWR	Writes host CPU device data into other CPU devices.	○	○	×
D.DDWR DP.DDWR		×	×	○
S.DDRD SP.DDRD	Reads other CPU device data into the host CPU devices.	○	○	×
D.DDRD DP.DDRD		×	×	○
S.GINT SP.GINT	Requests start up of other CPU interrupt programs.	○	○	×
D.GINT DP.GINT		×	×	○

○: Available, ×: Not Available

(Example) Using the S.DDWR instruction
The QCPU device data can be written to the Motion CPU devices.

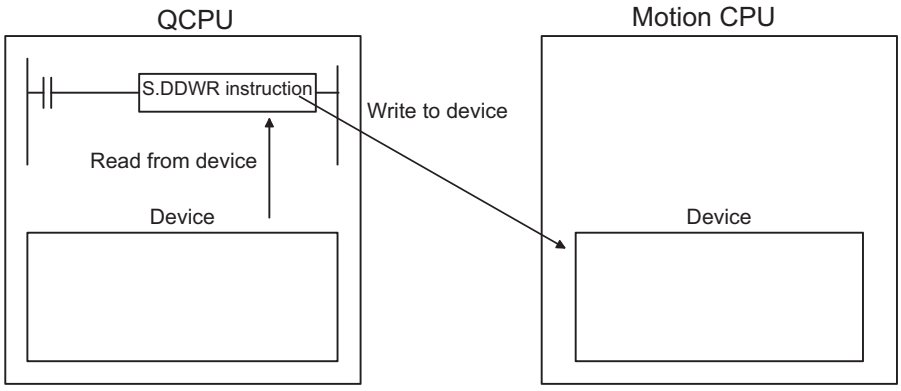


Diagram 4.24 Operation of S.DDWR instruction

POINT

One QCPU can concurrently issue up to 32 instructions of "Instructions dedicated to Motion CPU" and "Instructions dedicated to communication between multiple CPUs (except for S(P).GINT)".
Note that multiple instructions are executed in order starting from the first instruction.
When 33 or more incomplete instructions are identified, an "OPERATION ERROR (error code: 4107)" occurs.

Remark

Refer to the Motion CPU Manual for details on the use of the instructions dedicated to communication between multiple CPUs.

4.3.2 Start of interrupt program from QCPU to PC CPU module

The interrupt program from the QCPU to the PC CPU module can be started with the instructions dedicated to communication between multiple CPUs in Table 4.16.
(The interrupt program from the PC CPU module to other CPU module cannot be started.)

Table4.16 List of instructions dedicated to communication between multiple CPUs available for PC CPU module

Instruction name	Description
S.GINT SP.GINT	Requests start up of other CPU's interrupt programs.

(Example) When using the S.GINT instruction
The interrupt program from the QCPU to the PC CPU module can be started.

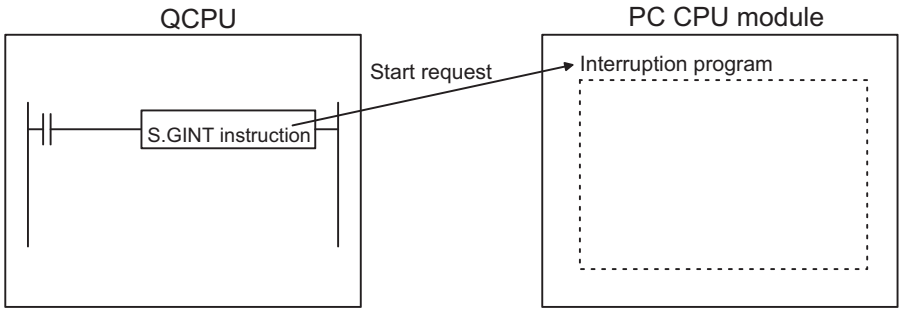


Diagram 4.25 Operation of S.GINT instruction

Remark

Refer to the PC CPU module Manual for details on the use of the instructions dedicated to communication between multiple CPUs.

4.4 Multiple CPU Synchronous Interrupt

The multiple CPU synchronous interrupt function executes interrupt programs (multiple CPU synchronous interrupt programs) at the timing of multiple CPU high speed transmission cycle.
The multiple CPU synchronous interrupt enables synchronization with multiple CPU high speed transmission cycle and communications among CPU modules.
Since the multiple CPU cycle is synchronized with the operation cycle of the Motion CPU, using the multiple CPU high speed transmission function together allows high-speed responses to requests from the Motion CPU and execution of sequence programs synchronized with the operation cycle.

(1) Multiple CPU synchronous interrupt programs

Multiple CPU synchronous interrupt programs are programs using interrupt pointer I45.
(A program from an interrupt pointer (I45) to the IRET instruction corresponds to a multiple CPU synchronous interrupt program.)
To execute multiple CPU synchronous interrupt programs, set interrupt permitted status with the EI instruction.

(2) Execution timing

Multiple CPU synchronous interrupt programs are executed at the timing of multiple CPU high speed transmission cycle.

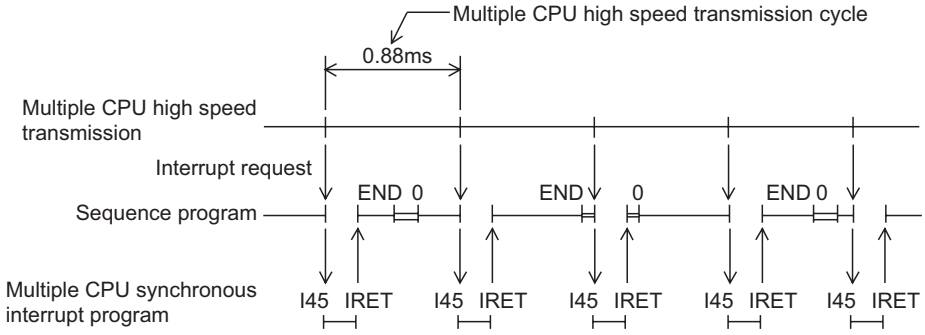


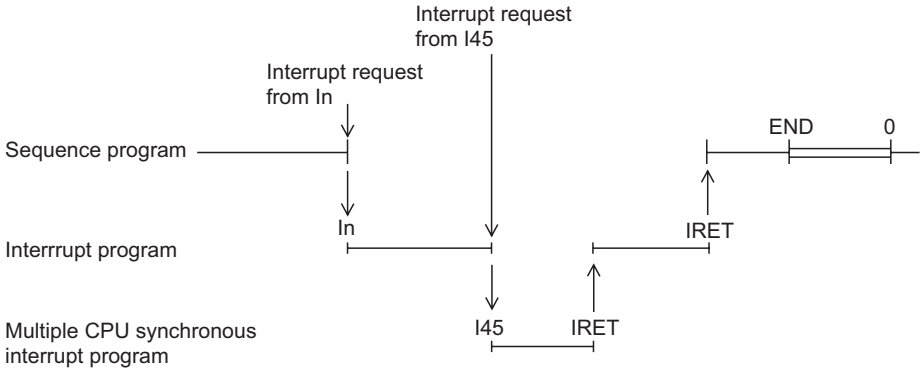
Diagram 4.46 Execution timing of multiple CPU synchronous interrupt program

POINT

The multiple CPU synchronous interrupt is available when the following CPU modules are used.

- Universal model QCPU (except Q02UCPU)
- Motion CPU (Q172DCPU, Q173DCPU)

When a multiple CPU synchronous interrupt factor occurs during the execution of another interrupt program, the running program is aborted to execute the multiple CPU synchronous interrupt program.



(3) Operation when the interrupt factor occurs

For operation when the interrupt factor occurs, refer to the following manual.

☞ QCPU User's Manual (Function Explanation, Program Fundamentals)

(4) Restrictions on creating the program

For the restrictions on creating the program, refer to the following manual.

☞ QCPU User's Manual (Function Explanation, Program Fundamentals)

4.5 Multiple CPU Synchronized Boot-up

Multiple CPU synchronized boot-up function synchronizes the start-ups of CPU No.1 to CPU No.4.
Since this function monitors the startup of each CPU module, when another station is accessed by manual operation, an interlock program which checks the CPU module startup is unnecessary.
With the multiple CPU synchronized boot-up function, the start-up is synchronized with the CPU module of slow start-up; therefore, the system start-up may be slow.

POINT

(1) Multiple CPU synchronized boot-up function is to access each CPU module in a multiple CPU system without an interlock.
This function is not for starting an operation simultaneously among CPU modules after start-up.

(2) The multiple CPU synchronized boot-up is available when the following CPU modules are used.
- Universal model QCPU (except Q02UCPU)
- Motion CPU (Q172DCPU, Q173DCPU)

(1) Multiple CPU synchronized boot-up setting

To use the multiple CPU synchronized boot-up function, check from No.1 to No.4 of Target PLC on Multiple CPU settings in PLC parameter of GX Developer.
"Synchronize Multiple CPU boot-up" is set to No.1 to No. 4 at default.

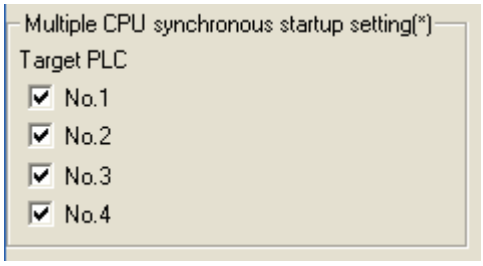


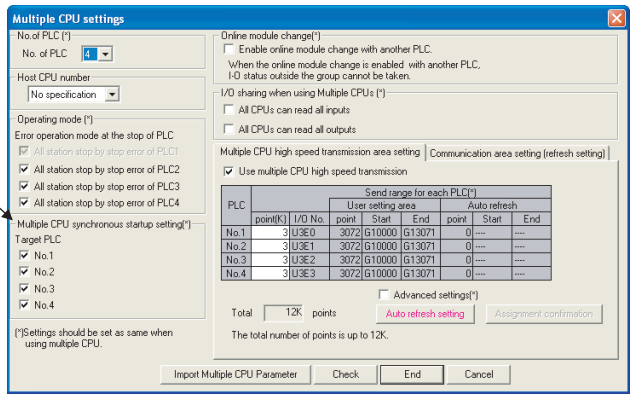
Diagram 4.25 Multiple CPU synchronized boot-up setting

Set the same Multiple CPU synchronous boot-up to all CPUs that constitute the Multiple CPU system.
When the all CPU modules that constitute the Multiple CPU system do not have the same setting, the stop error 3015 (the parameter setting mismatch error) will occur.

POINT

The CPU module other than the Universal model QCPU (Q03UDCPU, Q04UDHCPU, Q06UDHCPU) or Motion CPU (Q172DCPU and Q173DCPU) cannot execute the multiple CPU synchronized boot-up.
If the CPU module other than the Universal model QCPU (Q03UDCPU, Q04UDHCPU, Q06UDHCPU) or Motion CPU (Q172DCPU and Q173DCPU) is used, uncheck its CPU No.

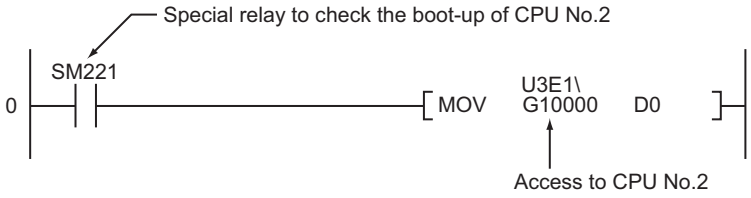
For a CPU module other than Universal model QCPUs (Q03UDCPU, Q04UDHCPU, and Q06UDHCPU) and Motion CPUs (Q172DCPU and Q173DCPU), remove the check mark.



Remark

When this function is not used (each CPU boot-up without synchronization), it is recommended to use SM220 to SM223 (Preparation completed flag of CPUs No.1 to No.4) of the special relay and create the sequence program to check the boot-up of the each CPU module.
[Program to check the boot-up of CPU No.2]

[Program to check the boot-up of CPU No.2]



CHAPTER5 PROCESSING TIME OF QCPU IN MULTIPLE CPU SYSTEM

5.1 Concept of Scan Time

The concept of scan time in the multiple CPU system is the same as that in the single CPU system.
This chapter describes how to calculate the processing time when the multiple CPU system is configured.

(1) I/O refresh time

I/O refresh time is calculated with the equation explained in the following manual.
☞QCPU User's Manual (Function Explanation, Program Fundamentals).
The I/O refresh time is prolonged by the following values when it is overlapped with bus access from/to other CPUs.

$$\text{(Extension time)} = \frac{\text{(No. of input points + No. of output points)}}{16} \times N3 \times \text{(No. of other CPUs) (μs)}$$

Use the value in Table5.1 for N3.

Table5.1 Extension of I/O refresh time

QCPU	N3	
	Systems with only a main base unit	Systems that include additional base units
Q00CPU	8.7μs	21μs
Q01CPU		
Q02CPU		
Q02HCPU, Q06HCPU, Q12HCPU, Q25HCPU		
Q12PHCPU, Q25PHCPU		
Q03UDCPU, Q04UDHCPU, Q06UDHCPU		

(2) Total value of instruction execution time

Refer to the following manual for details on the processing time of instructions dedicated to the multiple CPU system, and various processing times of instructions used in the multiple CPU system.
☞QCPU (Q mode)/QnACPU Programming Manual (Common Instructions)

(3) Common processing

The values in Table5.2 show the common processing time.

Table5.2 END processing time

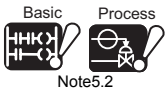
QCPU	Common processing time
Q00CPU	(0.05 to 0.13) × (No. of other CPUs)ms
Q01CPU	
Q02CPU	0.02ms
Q02HCPU, Q06HCPU, Q12HCPU, Q25HCPU	0.03ms
Q12PHCPU, Q25PHCPU	
Q02UCPU	0.02ms
Q03UDCPU	
Q04UDHCPU, Q06UHDCPU	

5.2 Factors for prolonged Scan Time

The processing time in Multiple CPU Systems is prolonged in comparison with Single CPU Systems when the following functions are used.
When using the following, add the values described later to the values calculated in Sections 5.1.

- Auto refresh of CPU shared memory (including multiple CPU high speed transmission function)
- Refresh of MELSECNET/G[Note5.1, Note5.2] and MELSECNET/H
- CC-Link automatic refresh

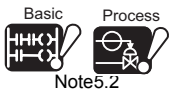
(1) Auto refresh of CPU shared memory (including multiple CPU high speed transmission function)



(a) Auto refresh of shared memory

The amount of time required to perform the refresh function set up with the Multiple CPU settings/multiple CPU high speed transmission area setting.
This value is the total amount of time required for writing into the host CPU's CPU shared memory, and the time required for reading from other CPUs' CPU shared memories.
These values are added when setting up the refresh settings/multiple CPU high speed transmission area setting with the PLC parameter "Multiple CPU settings."

The MELSECNET/G can only use the High Performance model QCPU whose first 5 digits of serial No. is 09012 or later.



The MELSECNET/G cannot use the Basic model QCPU or the Process CPU.

(b) Calculation of auto refresh time

The automatic refresh time of the CPU shared memory is calculated in the following equation.

1) For Basic model QCPU

(Auto refresh time)
= (N1 + (No. of transmission word points) × N2)) +
(N3 + (No. of other CPUs) × N4 + (No. of reception word points) × N5) (μs)

- The number of received words is the sum of the numbers of words transmitted by the other CPUs.

  (Example) When No. of CPU is set to 3 and the host CPU is CPU No. 1
  The number of received words is the sum of the numbers of words sent by CPUs No.2 to No.3.

- For N1 to N5, use the values in Table5.3.

Table5.3 Auto refresh time

Basic model QCPU	N1	N2	N3	N4	N5
Q00CPU	63μs	1.13μs	63μs	161μs	0.88μs
Q01CPU	57μs	1.03μs	57μs	146μs	0.80μs

2) For High Performance model QCPU/Process CPU

(Auto refresh time) = (N1 + (No. of reception word points) × N2) × (No. of other CPUs)
+ (N3 + (No. of transmission word points) × N4) (μs)

- The number of received words is the sum of the numbers of words transmitted by the other CPUs.

  (Example) When No. of CPU is set to 4 and the host CPU is CPU No. 1
  The number of received words is the sum of the numbers of words sent by CPUs No.2 to No.4.

- Use the values in Table5.4 for N1 to N4.

Table5.4 Auto refresh time

High Performance model QCPU/Process CPU Univwesal model QCPU	N1	N2	N3	N4
Q02CPU	82μs	0.52μs	106μs	0.17μs
Q02HCPU, Q06HCPU, Q12HCPU, Q25HCPU	27μs	0.44μs	27μs	0.08μs
Q12PHCPU, Q25PHCPU				

3) For Universal model QCPU

(Auto refresh time)
= (N1 + (No. of transmission word points) × N2)) +
(N3 + (No. of other CPUs) × N4 + (No. of reception word points) × N5) (μs)

- The number of received words is the sum of the numbers of words transmitted by the other CPUs.

  (Example) When No. of CPU is set to 4 and the host CPU is CPU No. 1. The number of received words is the sum of the numbers of words sent by CPUs No.2 to No.4.

- For the auto refresh using the multiple CPU high speed transmission area, use values in Table5.5 for N1 to N5.

Table5.5 Auto refresh time

Basic model QCPU	N1	N2	N3	N4	N5
Q02UCPU	-	-	-	-	-
Q03UDCPU	6μs	0.207μs	2μs	9μs	0.393μs
Q04UDHCPU,Q06UDHCPU	6μs	0.183μs	2μs	9μs	0.327μs

- For the auto refresh using the CPU shared memory , use values in Table5.5 for N1 to N5.

Table5.6 Auto refresh time

Basic model QCPU	N1	N2	N3	N4	N5
Q02UCPU	34μs	0.155μs	120μs	30μs	0.420μs
Q03UDCPU	9μs	0.162μs	28μs	21μs	0.410μs
Q04UDHCPU,Q06UDHCPU	8μs	0.132μs	25μs	20μs	0.410μs

(c) When auto refresh processing is duplicated with other CPU

The amount of time required for the auto refresh process will be prolonged by the following amount of time when processing is duplicated with the auto refresh function on other CPUs.

1) For Basic model QCPU

(Extension time) = 4 × (No. of reception word points) × N6 × (No. of other CPUs) (μs)

Use the values in Table5.7 for N6

Table5.7 Time prolonged when processing of other CPU is duplicated

Basic model QCPU	N6	
	System with main base unit only	System including extension base unit(s)
Q00CPU Q01CPU	0.54μs	1.30μs

2) For High Performance model QCPU/Process CPU

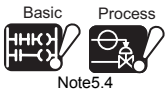
(Extension time) = (No. of transmission/reception word points) × N5 × (No. of other CPUs) (μs)

Use the values in Table5.8 for N5

Table5.8 Time prolonged when processing of other CPU is duplicated

High Performance model QCPU/Process CPU Univwesal model QCPU	N5	
	System with main base unit only	System including extension base unit(s)
Q02CPU Q02HCPU, Q06HCPU, Q12HCPU, Q25HCPU Q12PHCPU, Q25HCPU Q02UCPU Q03UDCPU,Q04UDHCPU, Q06UDHCPU	0.54μs	1.30μs

(2) Refresh of MELSECNET/G[Note5.3, Note5.4] and MELSECNET/H



(a) Refresh time of MELSECNET/G and MELSECNET/H

The amount of time required for performing the refresh between the QCPU and the MELSECNET/G or MELSECNET/H network module.
For refresh time of MELSECNET/G and MELSECNET/H, refer to the following manual.

☞ MELSECNET/G Network System Reference Manual
☞ Q Corresponding MESLECNET/H Network System Reference Manual

(b) Calculation of refresh time

The refresh time is prolonged by the following values when the refresh is requested from the MELSECNET/G or MELSECNET/H module of the other CPU at the same time.

1) For Basic model QCPU

(Extension time) = 4 × (No. of transmission/reception word points) × N6 × (No. of other CPUs) (μ s)

The number of transmission/reception words is the total number of transfer data below.

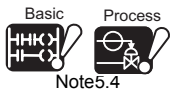
- Link refresh data : $\frac{(LB + LX + LY + SB)}{16}$ +LW+SW

Use the values in Table5.9 for N6

Table5.9 Time prolonged in simultaneous refresh request with the MELSECNET/H module of other CPU

Basic model QCPU	N6	
	System with main base unit only	System including extension base unit(s)
Q00CPU Q01CPU	0.54μs	1.30μs

The MELSECNET/G can only use the High Performance model QCPU whose first 5 digits of serial No. is 09012 or later.



The MELSECNET/G cannot use the Basic model QCPU or the Process CPU.

High Performance Note5.5

Process Note5.6

Universal Note5.7

2) For High Performance model QCPU[Note5.5]/Process CPU[Note5.6]/Universal model QCPU

(Extension time) = (No. of transmission/reception word points) × N5 × (No. of other CPUs) (μ s)

The number of transmission/reception words is the total number of transfer data below.

- Link refresh data : $\frac{(LB + LX + LY + SB)}{16}$ + LW+SW
- Data transferred to file register of memory card : $\frac{(LB + LX + LY + SB)}{16}$ + LW+SW
- Transfer between data links[Note5.7] : $\left(\frac{LB}{16} + LW\right) \times 2$

Use the values in Table5.10 for N5

Table5.10 Time prolonged when refresh is requested from MELSECNET/G or MELSECNET/H module at the same time

High Performance model QCPU/Process CPU Univwesal model QCPU	N5	
	System with main base unit only	System including extension base unit(s)
Q02CPU	0.54μs	1.30μs
Q02HCPU, Q06HCPU, Q12HCPU, Q25HCPU		
Q12PHCPU, Q25HCPU		
Q02UCPU		
Q03UDCPU, Q04UDHCPU, Q06UDHCPU		

High Performance Note5.5

The MELSECNET/G can only use the High Performance model QCPU whose first 5 digits of serial No. is 09012 or later.

Process Note5.6

The MELSECNET/G cannot use the Process CPU.

Universal Note5.7

Since the Universal model QCPU does not support transfer between data links, adding the number of points for transfer between data links is unnecessary.

(3) CC-Link auto refresh

(a) Auto refresh time on CC-Link network

The amount of time required for performing the refresh process between QCPU and CC-Link master local modules.

Refer to the following manual for details on the auto refresh time for CC-Link.

☞ QJ61BT11N CC-Link System Master Local Module User's Manual

(b) Calculation of auto refresh time

The amount of time required for the auto refresh process will be prolonged only by the following amount of time when requests for refreshing are issued by other CC-Link modules at the same time on a multiple CPU system.

(Extension time) = (No. of transmission/reception word points) × N5 × (No. of other CPUs) (μ s)

The number of transmission/reception words is the transfer data below.

・ Link refresh data : $\frac{(RX + RY + SB)}{16}$ + SW

Use the values in Table5.11 for N5

Table5.11 Time prolonged in simultaneous refresh request with the CC-Link module of other CPU

QCPU	N5	
	System with main base unit only	System including extension base unit(s)
Q00CPU	0.54μs	1.30μs
Q01CPU		
Q02CPU		
Q02HCPU, Q06HCPU, Q12HCPU, Q25HCPU		
Q12PHCPU, Q25HCPU		
Q02UCPU, Q03UDCPU, Q04UDHCPU, Q06UDHCPU		

5.3 Reducing processing time

(1) Multiple CPU system processing

Access is made between a CPU module and an I/O module or intelligent function module through a bus (base unit pattern, extension cable) and this bus cannot be used by multiple CPU modules at the same time.
If more than one CPU module attempt to use it simultaneously, the CPU module attempted access later is placed in "Standby" status until the processing of the first CPU module is completed.
In the multiple CPU system, this waiting time (time of "Standby status") will cause delay in input and output and increase in scan time.

(2) Maximum standby time

In the multiple CPU system, waiting time of the host CPU will reach the maximum when:

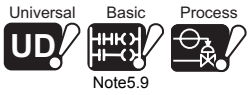
- Using the maximum number of CPU modules
- Using extension base unit(s)
- An intelligent function module on an extension base unit has high volume of data
- Simultaneous accesses are made to a module on the extension base unit where the maximum number of CPU modules is mounted.

(3) Reducing processing time for multiple CPU system

The following methods are available for reducing the processing time in the multiple CPU system.

- Place modules of high access points (e.g. MELSECNET/G, MELSECNET/H, or CC-Link) together on the main base unit.
- Set one QCPU as the control CPU to control the modules of high access points (e.g. MELSECNET/G, MELSECNET/H, or CC-Link) to prevent simultaneous access.
- Reduce the number of refresh points of the MELSECNET/G, MELSECNET/H, and CC-Link etc.
- Reduce the number of auto refresh points between CPU modules.

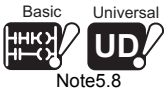
POINT



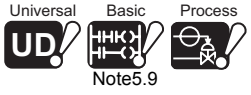
It is possible to reduce scan time by changing the following PLC parameter settings:

- A Series CPU compatibility setting *Note5.8*
- Floating point arithmetic processing *Note5.9*

☞ QCPU User's Manual (Function Explanation, Program Fundamentals).



For the Basic model QCPU and the Universal model QCPU, A series CPU compatibility setting cannot be made.



For the Basic model QCPU, the Process CPU or Universal model QCPU, the floating point calculation processing cannot be changed.

CHAPTER6 PARAMETER ADDED FOR MULTIPLE CPU SYSTEM

6.1 Parameter list

(1) Parameters that enable the use of multiple CPU system

Compared with the single CPU system, the multiple CPU system has additional settings of "No. of CPU", "control CPU", "refresh setting (auto refresh setting)" in PLC parameters.

The same PLC parameters must be set to all the CPU modules used in the multiple CPU system, except some settings.

When using a PC CPU module, reuse the multiple CPU system parameters in the PC CPU setting utility.

☞PC CPU module manual

(2) The PLC parameter settings for use in multiple CPU system

The necessity of setting PLC parameters and necessity of same setting that are required for using multiple CPU system are listed in Tables 6.1 and 6.2.

When parameters such as multiple CPU settings have been changed, make the same settings for all CPUs in the multiple CPU system, then reset CPU No.1 or reapply power to the multiple CPU system (power ON to OFF to ON).

It is possible to reuse the multiple CPU parameters set up for another project with GX Developer.

(Refer to Section 8.2.1 (4) and 8.2.2 (4) for reuse of the multiple CPU parameters.)

(a) For Basic model QCPU, High Performance model QCPU and Process CPU

The table 6.1 shows the PLC parameter settings that are required when the Basic model QCPU, the High Performance QCPU and the Process CPU are used.

Table6.1 Setting list for the multiple CPU and I/O Assignment

PLC parameter			Necessity of setup *1	Necessity of same setting *2	Reference
I/O assignment	I/O Assignment				QCPU User's Manual (Function Explanation, Program Fundamentals)
		Type	----	○	
		Model name	----	----	
		Points	----	○	
		StartXY	----	○	
	Base setting				
		Base model name	----	----	
		Power model name	----	----	
		Extension cable	----	----	
		slots	----	○	
	Switch settings		----	----	
	Detailed settings				
		Error time output mode	----	----	
		H/W error time PLC operation mode	----	----	
		I/O response time	----	----	
		Control PLC	○	○	Section 6.1.6
PLC system	Points occupied by empty slot		----	○	QCPU User's Manual (Function Explanation, Program Fundamentals)
Multiple CPU settings	No. of PLC		○	○	Section 6.1.1
	Operation mode		△	○	Section 6.1.2
	Online module change Note6.1		△	△	Section 6.1.3
	All CPUs can read all inputs		△	△	Section 6.1.4
	All CPUs can read all outputs		△	△	
	Refresh setting				Section 6.1.5
		Send range for each PLC	△	○	
		PLC side devices	△	----	

Basic High Performance Note6.1

*1:Necessity of setup column

○ : Items that must be set up for multiple CPU system (operations not possible if not set up.)

△ : Items that may be set up when required for multiple CPU system

---- : Items that are the same as single CPU system.

*2:Necessity of same setting column

○ : Items that must be the same settings for all CPU modules on the multiple CPU system.

△ : Items that must be the same settings for all QCPUs and PC CPU module on the multiple CPU system
(items that do not have settings for Motion CPUs).

---- : Items that can be setup up individually for each CPU modules on the multiple CPU system.

Basic High Performance Note6.1

For the Basic model QCPU, the online module change cannot be set.
For the High Performance model QCPU, modules cannot be changed online. To change a module online when using the Process CPU, set "Enable online module change".

(b) For Universal model QCPU

The table 6.2 shows the PLC parameter settings that are required when the Universal model QCPU is used..

Table6.2 Setting list for the multiple CPU and I/O Assignment

PLC parameter			Necessity of setup *1	Necessity of same setting *2	Reference
I/O assignment	I/O Assignment				QCPU User's Manual (Function Explanation, Program Fundamentals)
		Type	----	○	
		Model name	----	----	
		Points	----	○	
		StartXY	----	○	
	Base setting				
		Base model name	----	----	
		Power model name	----	----	
		Extension cable	----	----	
		slots	----	○	
	Switch settings		----	----	
	Detailed settings				
		Error time output mode	----	----	
		H/W error time PLC operation mode	----	----	
		I/O response time	----	----	
		Control PLC	○	○	Section 6.1.6
PLC system	Points occupied by empty slot		----	○	QCPU User's Manual (Function Explanation, Program Fundamentals)
Multiple CPU settings	No. of PLC		○	○	Section 6.1.1
	Operation mode		△	○	Section 6.1.2
	Multiple CPU synchronized boot-up		△	○	Section 6.1.7
	Online module change		△	○	Section 6.1.3
	All CPUs can read all inputs		△	△	Section 6.1.4
	All CPUs can read all outputs		△	△	
	Multiple CPU high speed transmission area setting				Section 6.1.8
		Multiple CPU high speed transmission function	○	○	
		CPU specific send range	○	○	
		Auto refresh			
		Number of points	△	○	
		Start	△	----	
		Advanced settings	△	○	
		Restricted system area *3	△	----	
	Refresh setting				Section 6.1.5
		Send range for each PLC	△	○	
		PLC side device	△	----	

*1:Necessity of setup column

○ : Items that must be set up for multiple CPU system (operations not possible if not set up.)

△ : Items that may be set up when required for multiple CPU system

---- : Items that are the same as single CPU system.

*2:Necessity of same setting column

○ : Items that must be the same settings for all CPU modules on the multiple CPU system.

△ : Items that must be the same settings for all QCPUs and PC CPU module on the multiple CPU system
(items that do not have settings for Motion CPUs).

---- : Items that can be setup up individually for each CPU modules on the multiple CPU system.

(3) Multiple CPU parameters check

At the time of the multiple CPU system power-on, reset or mode change from STOP to RUN of CPU No.1, or parameter change, whether the multiple CPU parameters are the same settings for all CPUs or not is checked as shown in Table 6.3 with items marked ○ and △ in the Necessity of same setting column in Tables 6.1 and 6.2 (Consistency check between CPU modules).

(a) When all CPUs are the same

The multiple CPU system will be started up.

(b) When all CPUs are not the same

The operations described in Table6.3 will be performed.
In this event, check the multiple CPU parameters, and set all CPUs with the same settings.
To start the multiple CPU system, reset CPU No.1 or turn off and on the multiple CPU system (power ON→OFF→ON).
(For the action after CPU No.1 reset, refer to Section 3.9.)

Table6.3 List of consistency check between CPUs

<table>
<tr><th colspan="2">Item</th><th>CPU No.1</th><th>CPU No.1 to 4</th></tr>
<tr><td colspan="2">When the multiple CPU system is powered on</td><td rowspan="2">No consistency check between CPU modules for the multiple CPU parameters will be run.*1</td><td rowspan="2">• A comparison check will be run on the multiple CPU parameters of CPU No.1.
• A "PARAMETER ERROR (error code: 3012/3015)" will occur in the host CPU if they do not match.</td></tr>
<tr><td colspan="2">When CPU No.1 is reset</td></tr>
<tr><td rowspan="3">• When the RUN/ STOP switch has been changed from STOP to RUN.
• When parameters are written with the GX Developer</td><td>When CPU in the RUN mode exist</td><td colspan="2">• A comparison check will be run on the multiple CPU parameters of RUN-state CPU of the lowest No.
• A "PARAMETER ERROR (error code: 3012/3015)" will occur in the host CPU if they do not match.</td></tr>
<tr><td>When CPUs in the RUN mode do not exist</td><td>• A comparison check will be run on the multiple CPU parameters of stopped CPU No.2.
• A "PARAMETER ERROR (error code: 3012/3015)" will occur in the host CPU if they do not match.</td><td>• A comparison check will be run on the multiple CPU parameters of CPU No.1.
• A "PARAMETER ERROR (error code: 3012/3015)" will occur in the host CPU if they do not match.</td></tr>
<tr><td>When a stop error occurs at CPU No.1</td><td>----</td><td>STOP to RUN is not allowed as a "MULTI CPU DOWN (error code: 7000)" error will occur in the host CPU. No consistency check between CPU modules.</td></tr>
</table>

* 1: The Universal model QCOU checks consistency of multiple CPU parameters among the CPU modules
A "PARAMETER ERROR (error code: 3015)" will occur in the host CPU if they do not match.

POINT

After multiple CPU system parameters unavailable with the Motion CPU are changed for the QCPU or PC CPU module in a multiple CPU system including a Motion CPU, be sure to reset the QCPU for CPU No.1 or turn off and on the PLC system.
Otherwise the QCPU or PC CPU module checks consistency between CPU modules with multiple CPU system parameters of the Motion CPU, causing a "PARAMETER ERROR (error code: 3012)."

6.1.1 Number of CPUs setting

(1) No. of PLC

The number of CPU modules to be used on a multiple CPU system are set at the PLC parameter's "Multiple CPU settings" screen in the (PLC) Parameter dialog box.

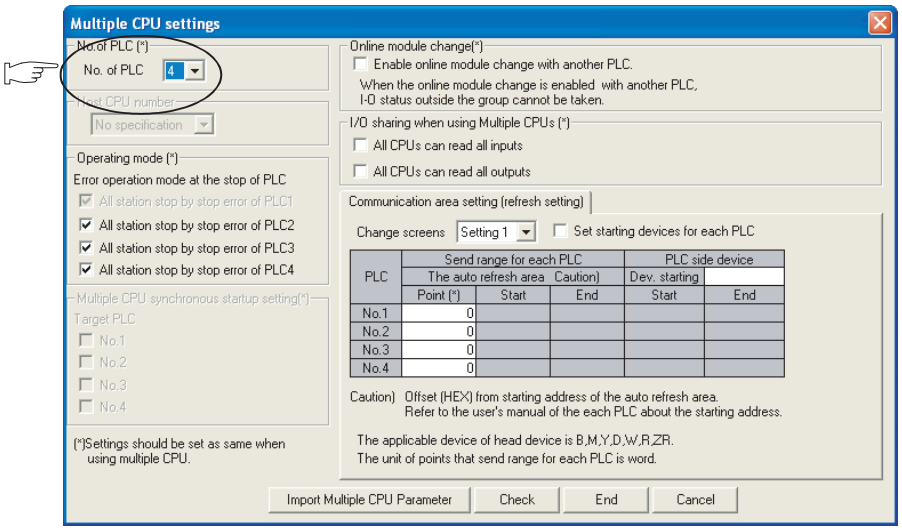


Diagram 6.1 No. of CPUs setting screen

(2) Reserving empty slot

When an empty slot is reserved for the purpose of mounting additional CPU modules in the future, set "PLC (Empty)" on the "I/O assignment" tab screen in the "(PLC) Parameter" dialog box.

For example, when setting "4" as "No. of CPUs" in use of High Performace model QCPU and reserving one of them for future use, set "CPU (Empty)" to slot 3.

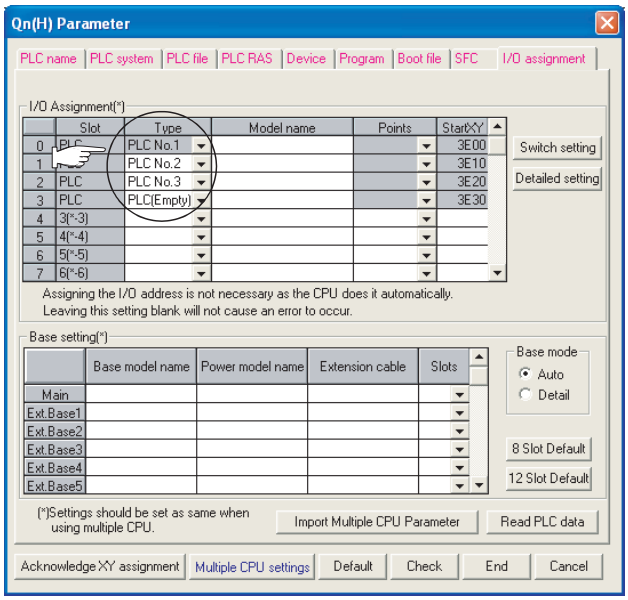


Diagram 6.2 Empty slot setting screen

POINT

In the mounted CPU module of CPU No.1, errors occur caused by the following error factors (1) or (2).

(1) When the number of mounted CPU modules exceeds the number set with the No. of CPU settings
  (a) When CPU No.1 is Basic model QCPU/Universal model QCPU
    CPU LAY ERROR (error code: 7030) occurs.
  (b) When CPU No.1 is High Performance model QCPU or Process CPU
    PARAMETER ERROR (error code: 3010) occurs.

(2) When CPU modules of which numbers are set in the No. of CPU setting are not mounted in the CPU module mounting slots
  (a) When CPU No.1 is Basic model QCPU/Universal model QCPU
    CPU LAY ERROR (error code: 7031) occurs.
  (b) When CPU No.1 is High Performance model QCPU or Process CPU
    PARAMETER ERROR (error code: 3010) occurs.

6.1.2 Operating mode setting

This is set to continue operation of other CPUs where a stopping error has not occurred when an error occurs at other than CPU No.1.
The operating mode for the CPU No.1 cannot be changed (all CPUs will suspend operations when a stop error is triggered for the CPU No.1.)
☞ Section 3.10

Basic Note6.2
High Performance Note6.2
Universal Note6.2

6.1.3 Online module change setting

This setting allows modules to be replaced online when the Process CPU is used.
☞ QCPU User's Manual (Hardware Design, Maintenance and Inspection)

6.1.4 I/O settings outside of the group

This is set when the input and output (X, Y) for I/O modules and intelligent function modules being controlled by other CPUs is to be downloaded to the host CPU.
☞ Section 3.4.2

6.1.5 Refresh setting

This is set up to automatically refresh the device data on the multiple CPU system.
☞ Section 4.1.2

Basic High Performance Universal Note6.2

For the Basic model QCPU and the Universal model QCPU (Q02UCPU), the online module change cannot be set.
For the High Performance model QCPU and the Universal model QCPU (except Q02UCPU), modules cannot be replaced online. To replace modules online when using the Process CPU, set [Enable online module change]..

6.1.6 Control CPU settings

Sets up the control CPUs (Control PLCs) for the I/O modules and intelligent function modules mounted on the base unit in the multiple CPU system.
All default settings are set to CPU No.1.

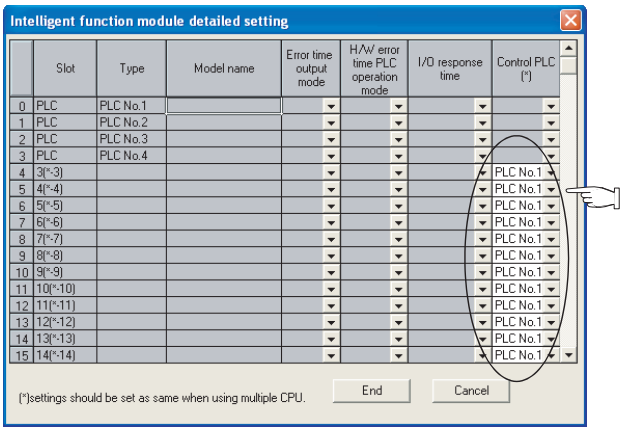


Diagram 6.3 Control CPU setting screen

6.1.7 Multiple CPU synchronized boot-up

This is set for synchronizing the boot-up time for each CPU module.
(☞Section 4.5)

6.1.8 Multiple CPU high speed transmission area setting

This is set when the auto refresh is performed using the multiple CPU high speed transmission area in the multiple CPU system.
(☞Section 4.4)

POINT

The multiple CPU synchronized boot-up and the multiple CPU high speed transmission area setting are available when the following CPU modules are used.

- Universal model QCPU (except Q02UCPU)
- Motion CPU (Q172DCPU, Q173DCPU)

CHAPTER7 PRECAUTIONS FOR USE OF AnS/A SERIES MODULE

7.1 Precautions for use of AnS/A series compatible module

(1) Available I/O modules and special function modules

When the multiple CPU system is configured with the High Performance model QCPU, AnS/A series compatible I/O modules and special function modules can be used.

When the Process CPU is used together, use of the AnS/A series compatible modules is not allowed.

(2) Setting of control CPU

The AnS/A Series compatible I/O modules or special function modules can be controlled by only one CPU (control CPU) of High Performance QCPUs No.1 to No.4 when configuring a multiple CPU system.

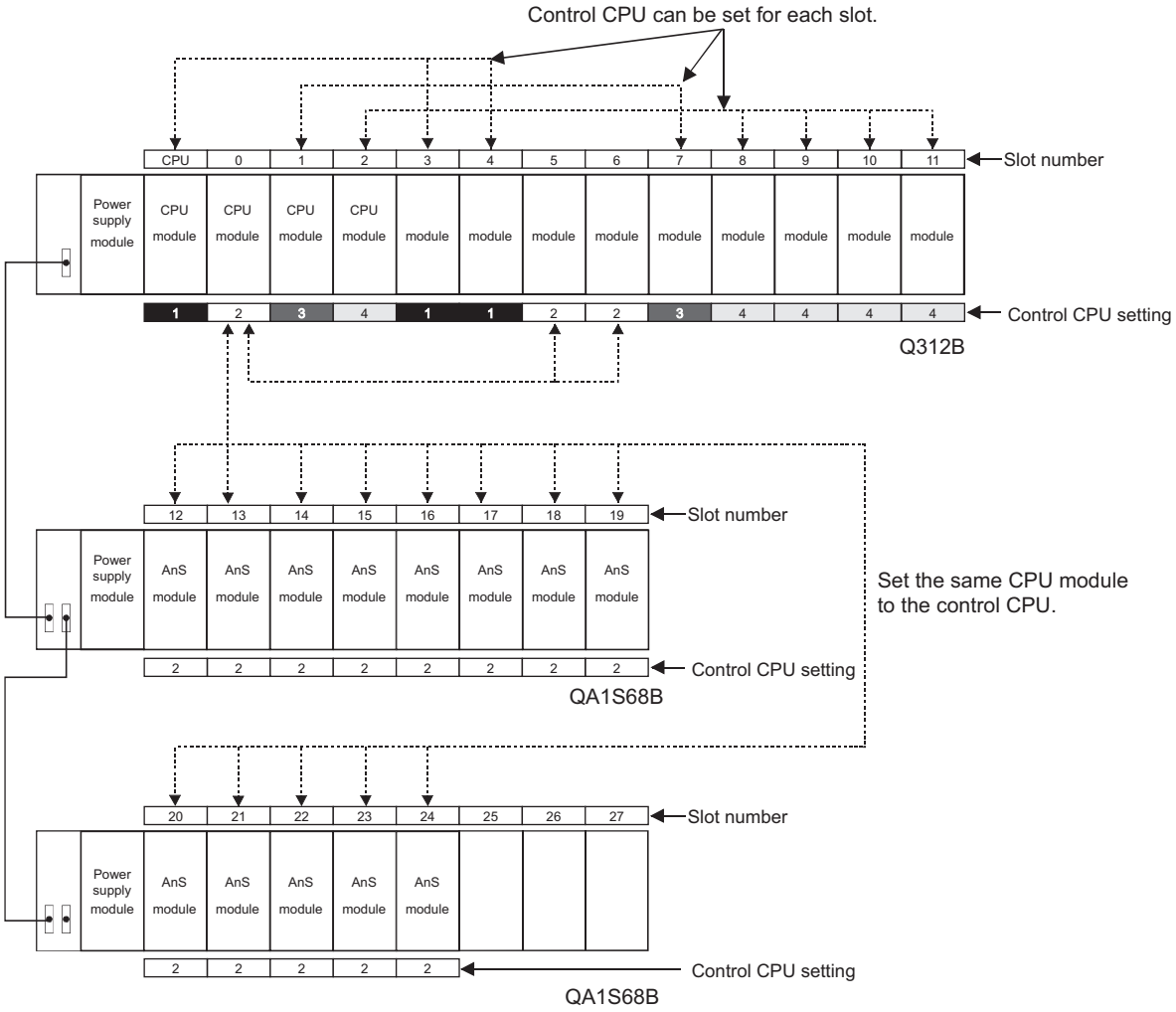
The following CPU module cannot be set as the control CPU for the I/O module and special function module that are compatible with the AnS/A series.

- Universal model QCPU
- Basic model QCPU
- Process CPU
- Motion CPU
- PC CPU module

(Example) When the control CPU is setup for CPU No.2

Every slot's control CPU on which I/O modules and special function modules compatible with the AnS/A Series are mounted is set to CPU No.2.

The "PARAMETER ERROR (error code: 3009)" occurs even if only one AnS/A Series compatible I/O module or special function module has another control CPU setting, the multiple CPU system will not be started up.



The control CPU setting shown in the illustration represents the following:

CPU module 1 to 4 :CPU number

(AnS/A) module 1 to 4 :Control CPU's CPU number

Diagram 7.1 Control CPU setting example for AnS/A compatible module

(3) Ranges of access to controlled and non-controlled modules

Table7.1 indicates access range to the controlled and non-controlled modules in the multiple CPU system.

Table7.1 Access range to controlled module and non-controlled module

Access target		Controlled module	Non-controlled module (I/O setting outside of the group)	
			Disabled (Not checked)	Enabled (Checked)
Input (X)		○	×	×
Output (Y)	Read	○	×	×
	Write	○	×	×
Buffer memory	Read	○	×	×
	Write	○	×	×

○ : Accessible × : FInaccessible

(4) Precautions for use of AnS/A series compatible modules

(a) Accessible device range

When the AnS series special-function modules shown in Table7.2 are used, a limitation is given to an accessible device range.

- A1SD51S, AD51-S3, AD51H-S3 type intelligent communication module

Table7.2 List of accessible device ranges

Device	Accessible device range
Input (X), Output (Y)	X/Y0 to 7FF
Internal relay (M), Latch relay (L)	M0 to 8191
Link relay (B)	B0 to FFF
Timer (T)	T0 to 2047
Counter (C)	C0 to 1023
Data register (D)	D0 to 6143
Link register (W)	W0 to FFF
Annunciator (F)	F0 to 2047

(b) Unavailable modules

The modules shown in Table7.3 cannot be used.

Table7.3 List of unavailable modules

Module Name	Type
MELSECNET/IO network module	A1SJ71LP21,A1SJ71BR11,A1SJ71QLP21, A1SJ71QLP21S,A1SJ71QLP21GE,A1SJ71QBR11, AJ71LP21,AJ71LP21G,AJ71BR11,AJ71LR21, AJ71QLP21,AJ71QLP21S,AJ71QLP21G, AJ71QBR11,AJ71QLR21
MELSECNET (II), /B data link module	A1SJ71AP21,A1SJ71AR21,A1SJ71AT21B, AJ71AP21,AJ71AP21-S3,AJ71AR21,AJ71AT21B
Ethernet interface module	A1SJ71QE71-B2-S3(-B5-S3), A1SJ71E71-B2-S3(-B5-S3) AJ71QE71N(-B5T),AJ71E71-B2(-B5T)
Serial communication module, computer link module	A1SJ71QC24(N),A1SJ71UC24-R2(-PRF), AJ71QC24N(N),AJ71QC24N-R2(-R4),A1SJ71UC24, AJ71UC24
CC-Link master-local module	A1SJ61QBT11,A1SJ61BT11,AJ61QBT11,AJ61BT11
Modem interface module	A1SJ71CMO-S3
ME-NET interface module	A1SJ71ME81

(c) Modules that require instruction rewriting

Dedicated instructions included in the QnA/A series program instructions cannot be used for modules shown in Table7.4.
Rewriting them using the FROM/TO instruction is required.

Table7.4 List of modules that require instruction rewriting

Module Name	Type
High speed counter module	A1SD61,A1SD62,A1SD62D(-S1), A1SD62E,AD61,AD61S1
MELSECNET/MINI-S3	A1SJ71PT32-S3,A1SJ71T32-S3
Positioning module	A1SD75P1-S3(P2-S3/P3-S3), AD75P1-S3(P2-S3,P3-S3)
ID module	A1SJ71ID1-R4,A1SJ71ID2-R4

(d) Modules which can use multidrop link function only

The computer link/multidrop link module A1SJ71UC24-R4 can use the multidrop link function only. Computer link function and printer function are not available.

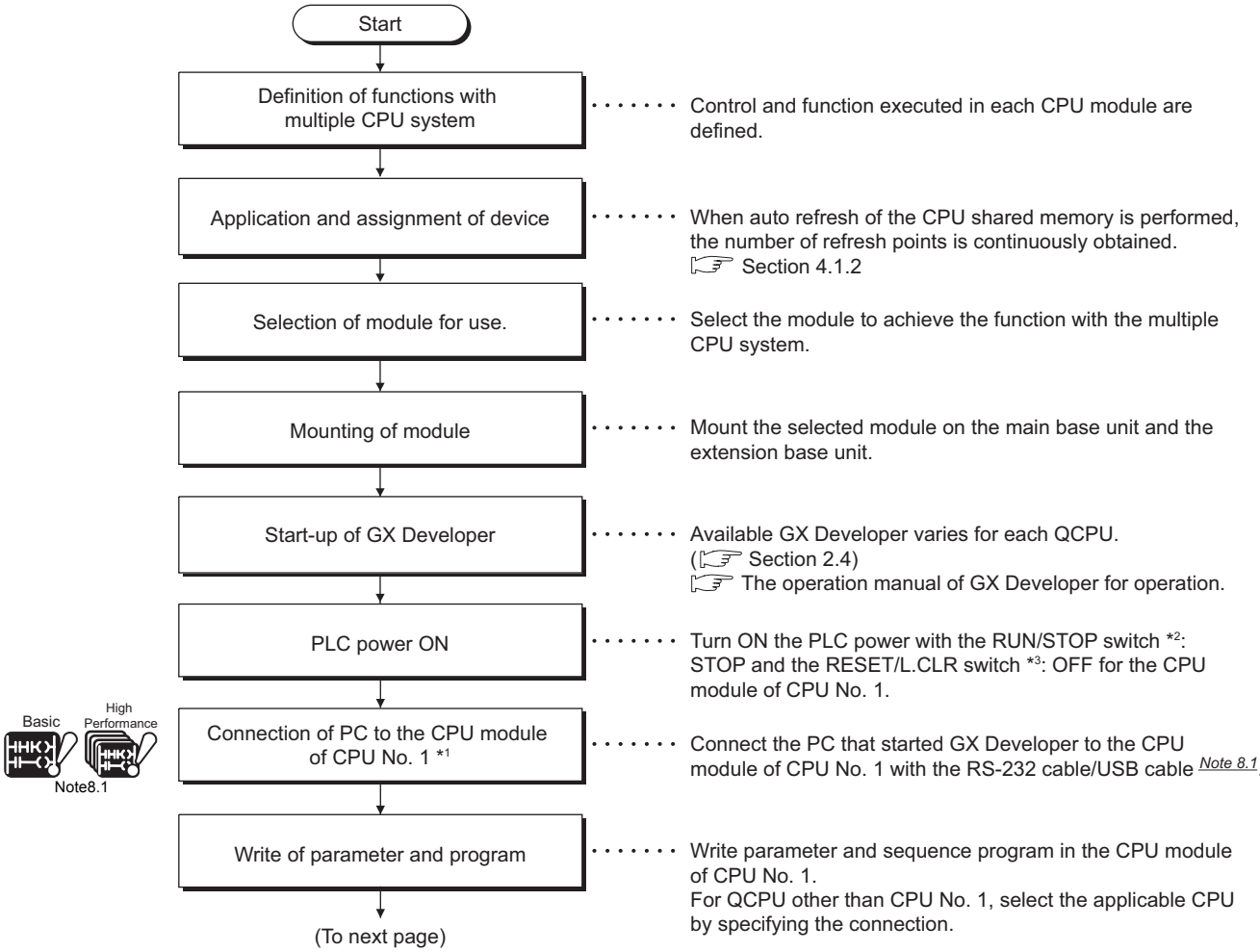
CHAPTER8 STARTING UP THE MULTIPLE CPU SYSTEM

This Chapter explains the standard start-up procedures for the multiple CPU system.

8.1 Flow-chart for Starting Up the Multiple CPU System

Parameters should be preset and sequence programs should be prepared in advance.
(☞ Section 8.2,Section 8.3)

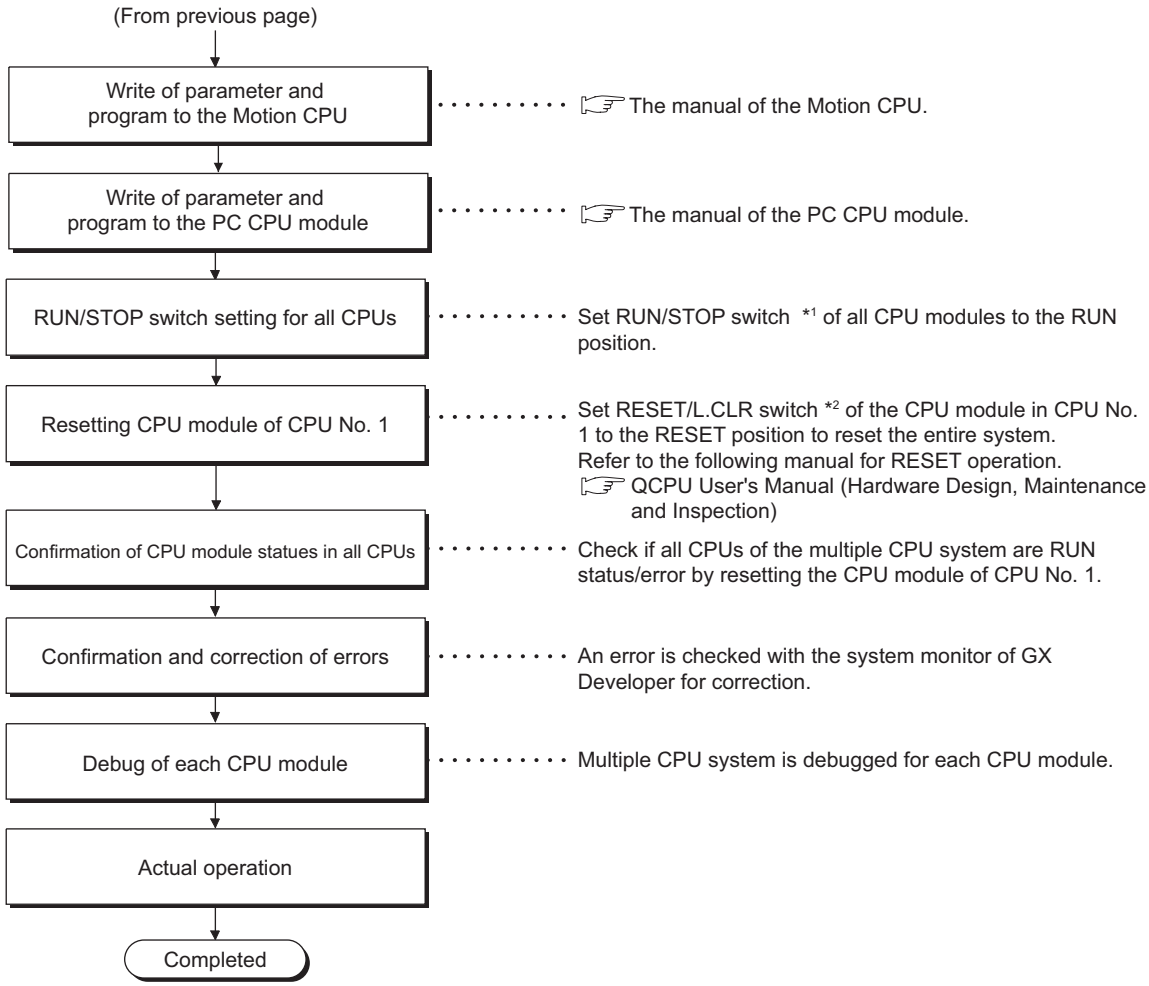
For settings of the Motion CPU and the PC CPU and creation of the program, refer to the manual of each CPU module.



* 1: When the PC CPU module is used, the QCPU can be connected to GX Developer through a bus cable by installing GX Developer into the PC CPU module.
☞ GX Developer operating manual.
* 2: For the Basic model QCPU and Universal model QCPU, it is the RUN/STOP/RESET switch.
* 3: For the Basic model QCPU and Universal model QCPU, it is the RUN/STOP/RESET switch.

Basic High Performance Note8.1

For the Basic modPel QCPU, USB cables are not usable.
For the Q02CPU, USB cables are not usable.



* 1: For the Basic model QCPU and Universal model QCPU, it is the RUN/RESET/STOP switch.
For the Motion CPU and the PC CPU module, refer to the manual of each CPU module.
* 2: For the Basic model QCPU and Universal model QCPU, it is the RUN/RESET/STOP switch.

Diagram 8.1 Procedure to start multiple CPU system

8.2 Setting Up the Multiple CPU System Parameters

This section explains the procedures for setting up the multiple CPU system parameters with GX Developer.
Refer to the GX Developer's operation manual for details on setting up all other parameters.

8.2.1 Parameter setting for the Basic model QCPU,High Paformance model QCPU,ProCess CPU

(1) System configuration

Diagram 8.2 shows an example procedures for setting up the multiple CPU system parameters.

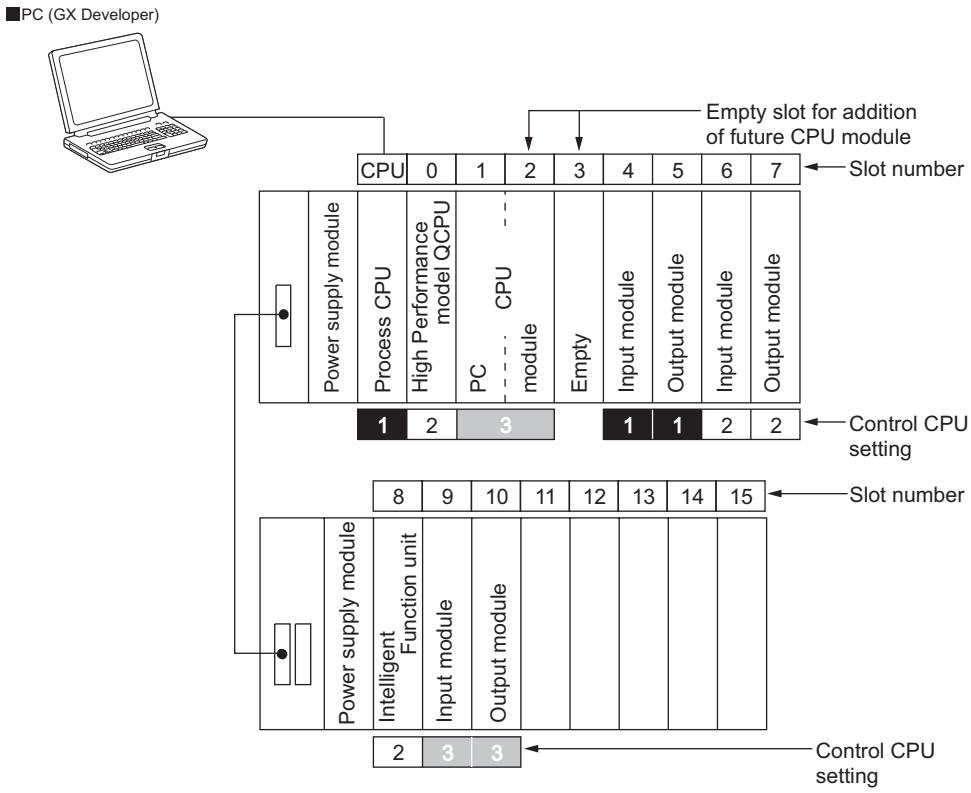
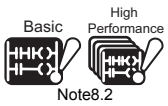


Diagram 8.2 Configuration example of multiple CPU system

(2) Parameters required for multiple CPU system

When the multiple CPU system is used, the following parameter settings are required. Parameters of "Same setting items for each CPU module" should be set with the same settings in all CPU modules used in the multiple CPU system except some parts.(☞ Section 6.1)



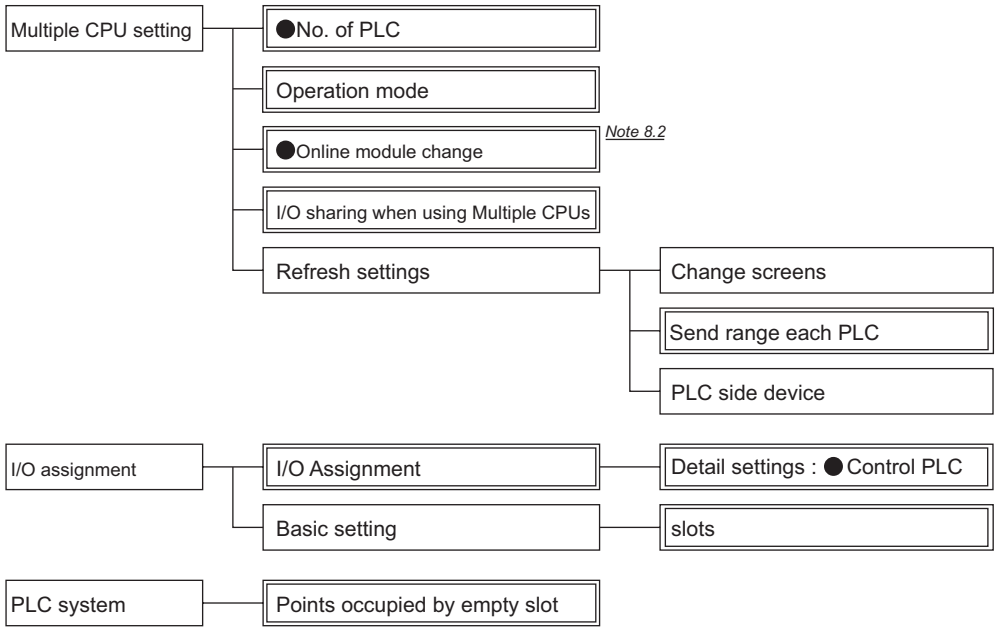
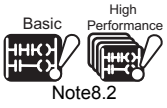
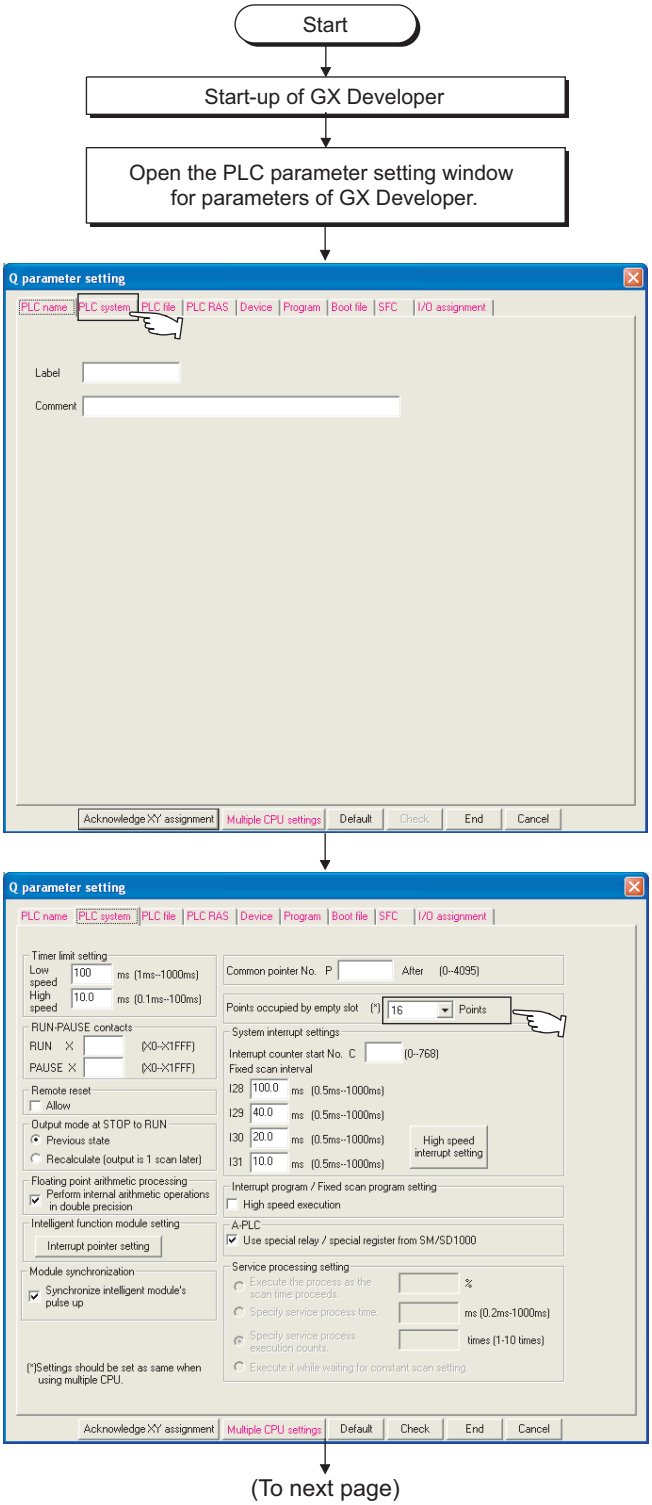


Diagram 8.3 List of parameters required for multiple CPU system



For the Basic model QCPU, the online module change setting is not available.
For the High Performance model QCPU, modules cannot be replaced online. To replace a module online when using the Process CPU, set "Enable online module change".

(3) When creating a new multiple CPU system



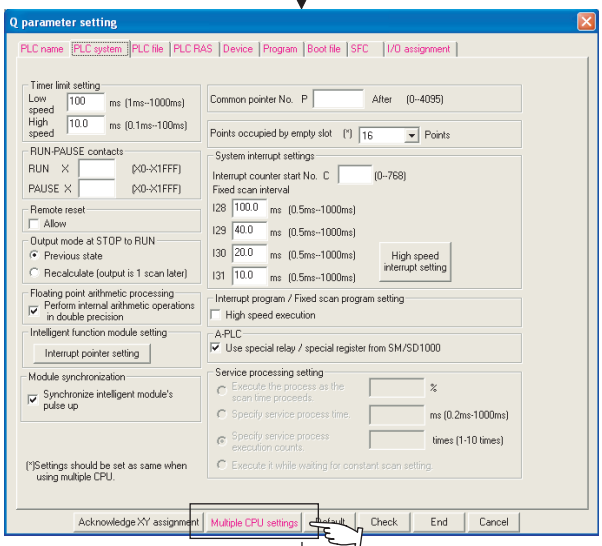
☞ The operating manual of GX Developer.

☞ The operating manual of GX Developer.

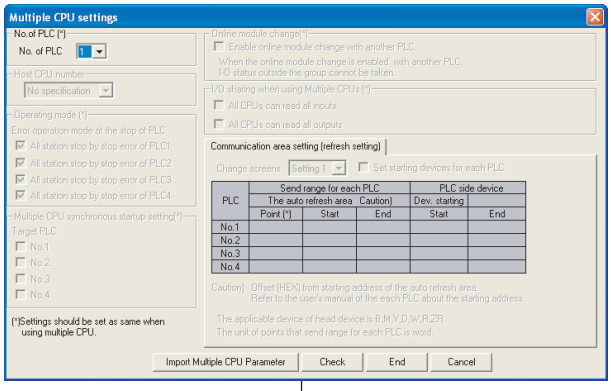
Select "PLC system" and display the PLC system setting window.

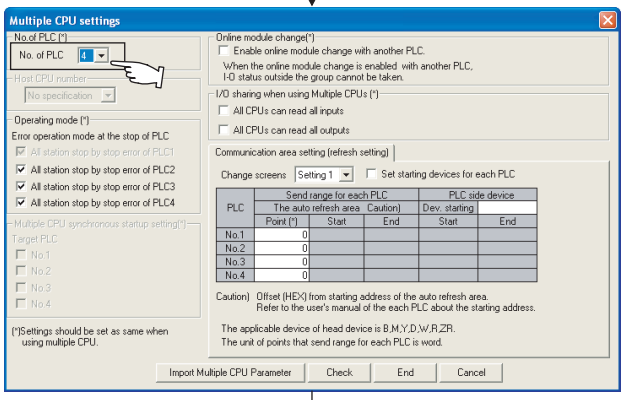
Points occupied by empty slot (Option)
· Set the occupied points for one empty slot.
Default: 16 points

(From previous page)



Select "Multiple CPU settings" and display the multiple CPU setting window.





Basic
Note8.3

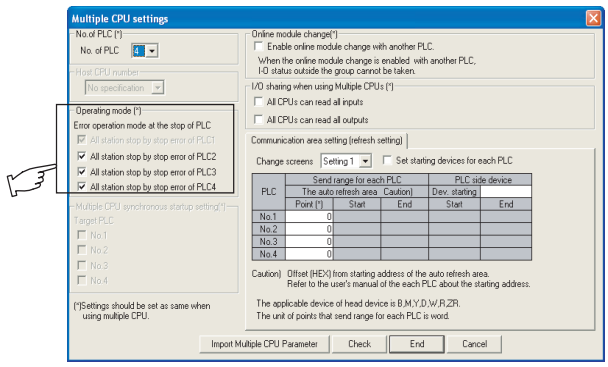
No. of PLC (mandatory item)
· Set the number of CPU modules mounted on the main base unit with the multiple CPU system. *Note 8.3*

(To next page)

Basic
Note8.3

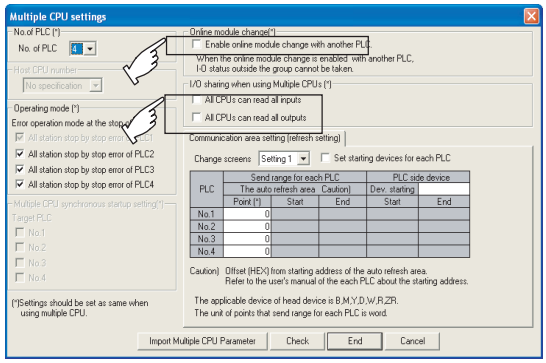
Since the number of CPU modules that can be mounted is up to 3 when using the basic model QCPU, do not set to "4".

(From previous page)



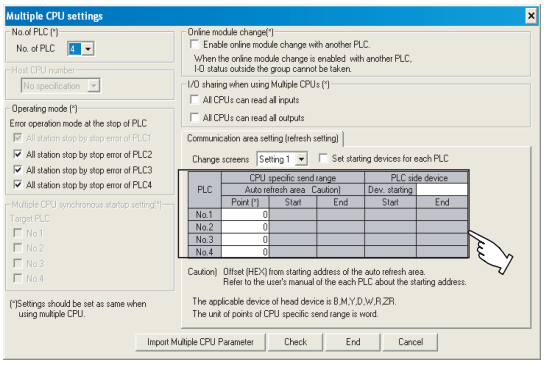
Operating mode (option)
- Select if all CPUs are stopped/operated for occurrence of stop error.
  Default: With any error of CPUs 2, 3 and 4, all CPUs stop (checked).
- For example, when "All station stop by stop error of PLC 2" is unchecked, other CPUs continue operation for an error of CPU No. 2.
- Operation of CPU No. 1 cannot be changed.

Basic High Performance Note8.4



Online module change Note 8.4/I/O sharing when using Multiple CPUs (option)
- Select if the online module change is set or if input/output outside of group is set.
  Default: Online module change setting (checked)
- Online module change is inhibited for the following cases.
  Online module change is not performed.
  I/O sharing when using Murtiple CPUs is performed.

I/O sharing when using Multiple CPUs
- Set if the input/output status beyond control of input/output setting outside of group is loaded or not.
  Default: Not loaded. (Not checked)



Communication area setting(refresh settings) (Option)
- Set the devices, used for data communications with auto refresh between CPU modules and the points of the auto refresh area.
- Use the points of the auto refresh area from the set startive device number.
- The number of points in the table below is occupied with one point in the auto refresh area.

Device	Occupied points
B,M,Y	16 points
D,W,R,ZR	1 point

(To next page)

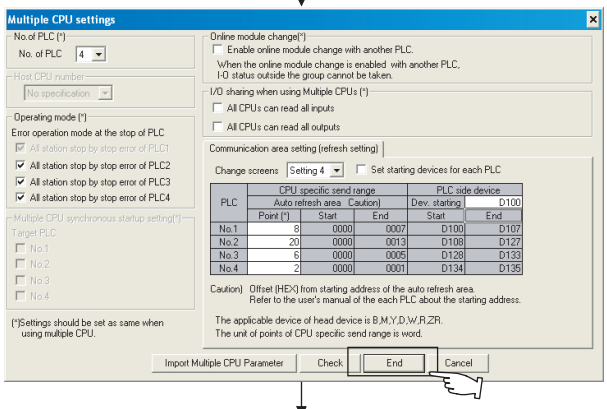
POINT

When replacing a module online, set all CPU modules on the multiple CPU system to "Enable online module change".

Basic High Performance Note8.4

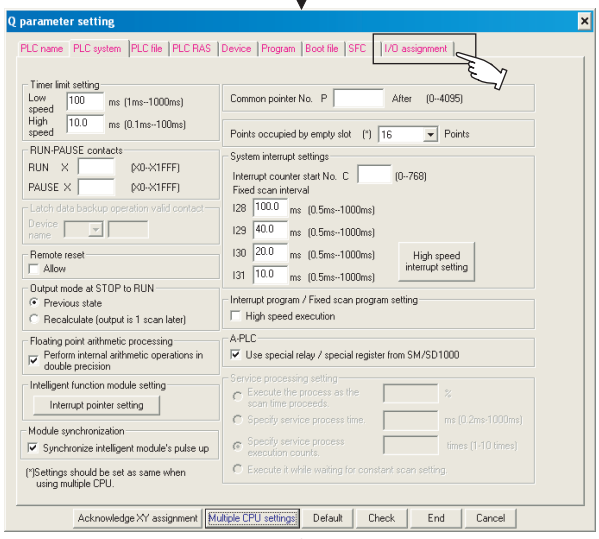
For the Basic model QCPU, the online module change setting is not available.
For the High Performance model QCPU, modules cannot be replaced online. To replace a module online when using the Process CPU, set "Enable online module change".

(From previous page)

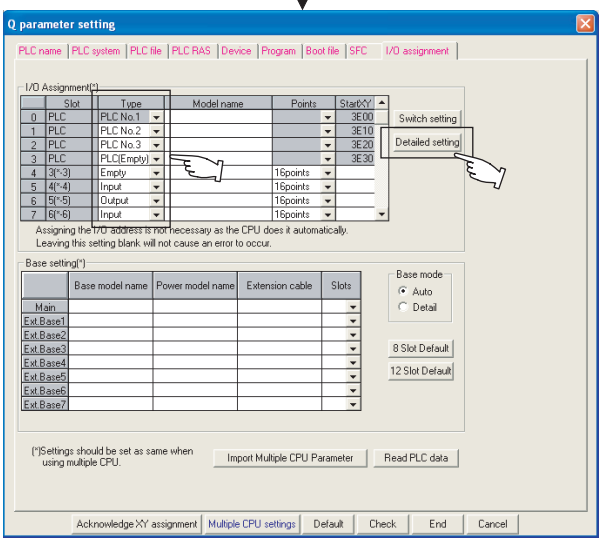


Refresh settings (option)

- With change of settings, 4 settings from setting 1 to setting can be made.
- After setting, select "Setting completed" and close the multiple CPU setting window.



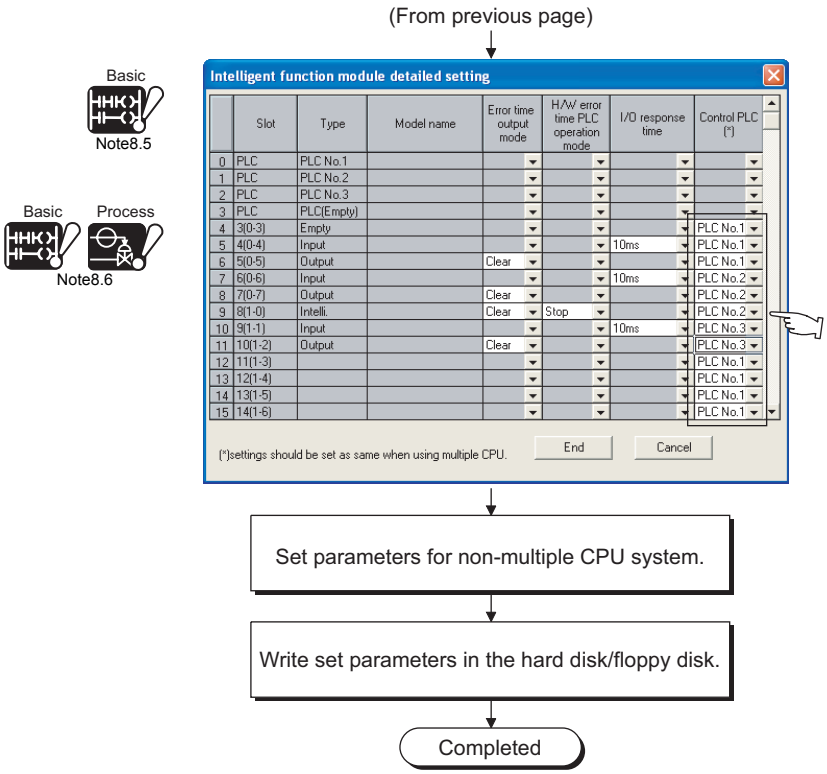
Select "I/O assignment" and display the I/O assignment setting window.



I/O assignment (option)

- Select the slot to "PLC (empty)" that does not mount the CPU module for each type.
- Select the type of each module from the pulldown menu.
- Select "Detailed setting" on the I/O assignment setting window and display the detail setting window.

(To next page)



Control PLC (mandatory item)

- Select control CPU (PLC No. 1 to PLC No. 4) for each slot. *Note 8.5*
- For the intelligent function module of function version A, the control CPU is set to PLC No. 1.
- For the AnS/A series compatible I/O module and special function module, the same High Performance model QCPU is set to the control CPU. *Note 8.6*

Diagram 8.4 Parameter setting procedure for new multiple CPU system creation

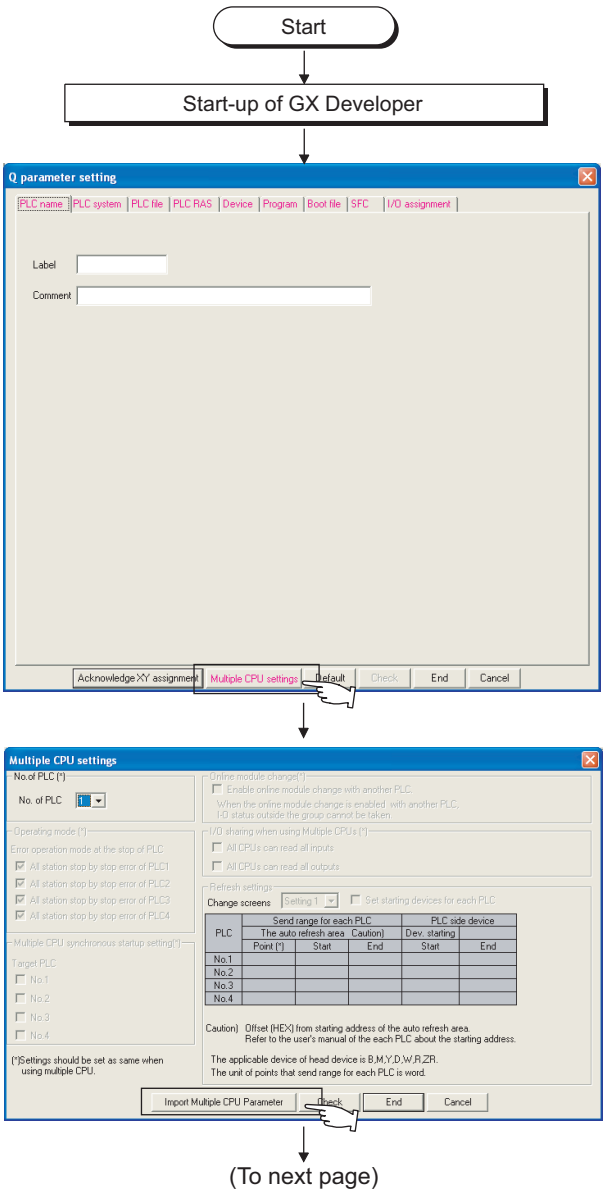
Basic
Note8.5

Since the number of CPU modules that can be mounted is up to 3 when using the basic model QCPU, do not select "PLC No.4".

Basic Process
Note8.6

For the Basic model QCPU or the Process CPU, using the AnS/A series compatible I/O modules and special function modules is not allowed.

(4) Reusing preset multiple CPU parameters

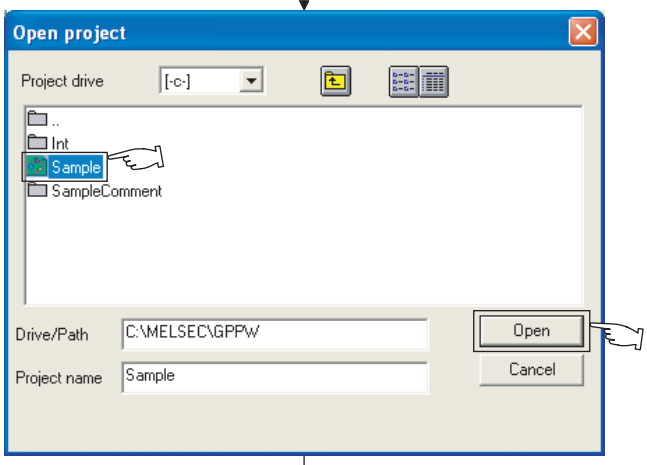


☞Refer to the operating manual of GX Developer.

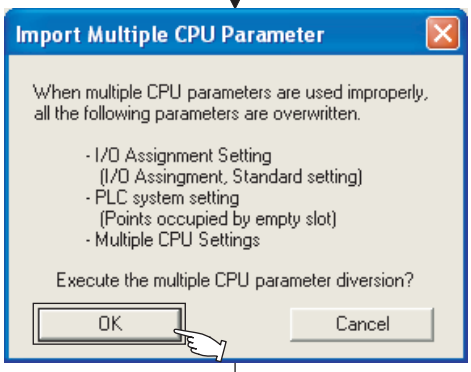
Open the PLC parameter setting window for the parameter of GX Developer.
Select "Multiple CPU settings" and display the multiple CPU setting window.

Carry-over of multiple CPU setting
· Click "Import Multiple CPU Parameter".

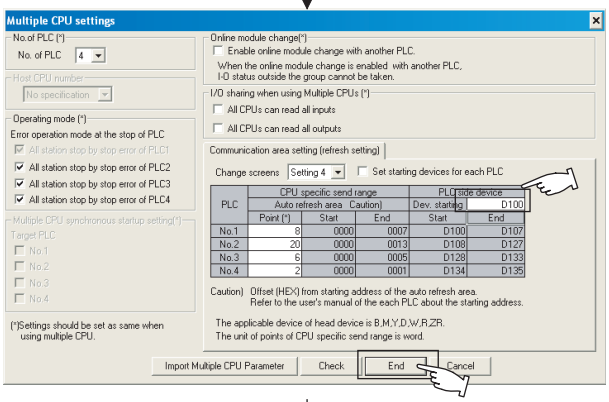
(From previous page)



Setting of carry-over project
- Select the project that carries over multiple CPU setting and I/O assignment.
- Click "Open".



When "OK" is selected, the multiple CPU setting and the I/O assignment setting data are read from the specified project and the data is overwritten.



Check the multiple CPU settings.
When the CPU device for refresh setting is changed, input the device number after change.
(Items with * should have the same settings for each CPU module.)

After checking the multiple CPU settings or completion of correction, select "END" and close the multiple CPU setting window.

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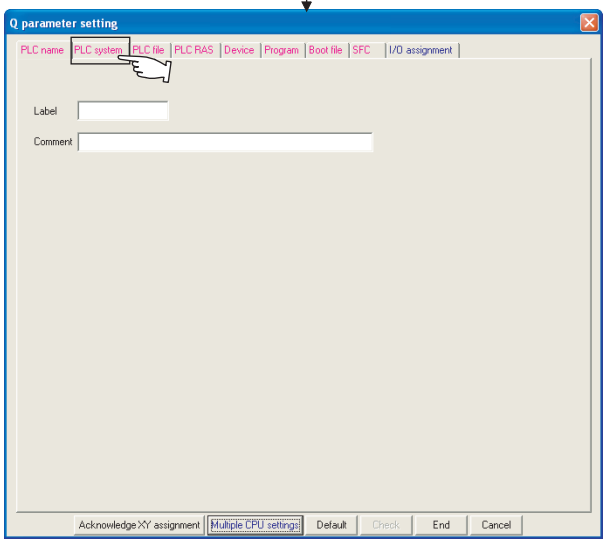
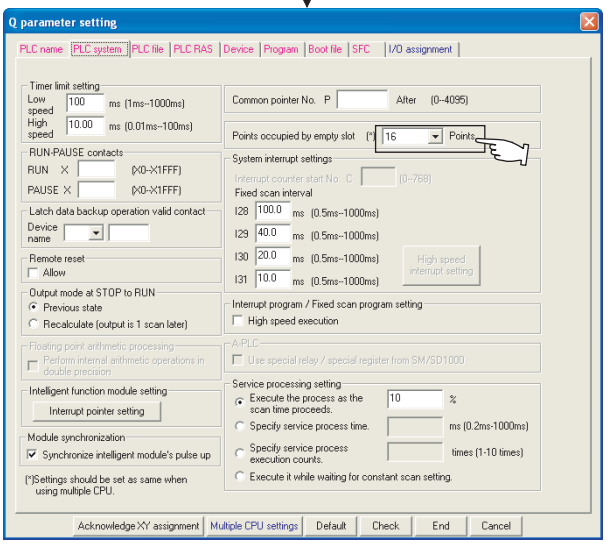


Select "PLC system" and display the PLC system setting window.



Check the empty slot points on the PLC system setting window.

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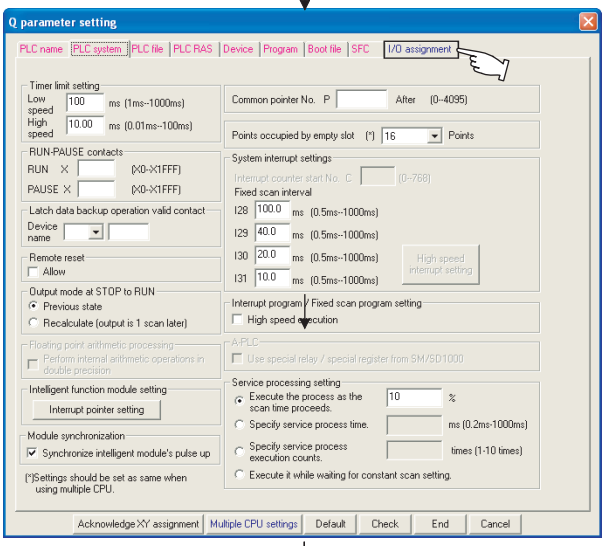
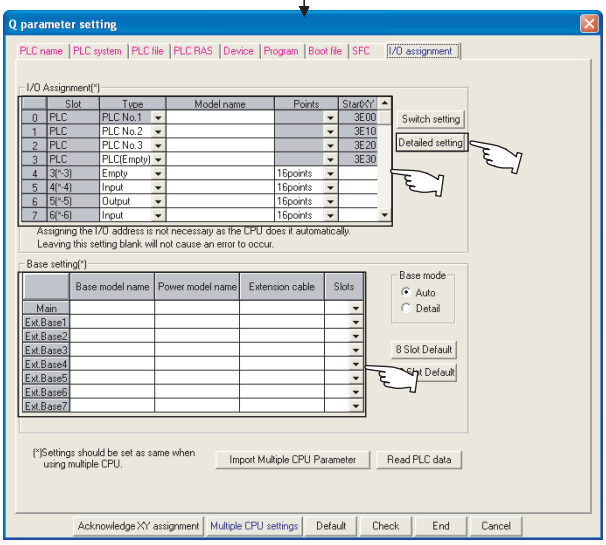
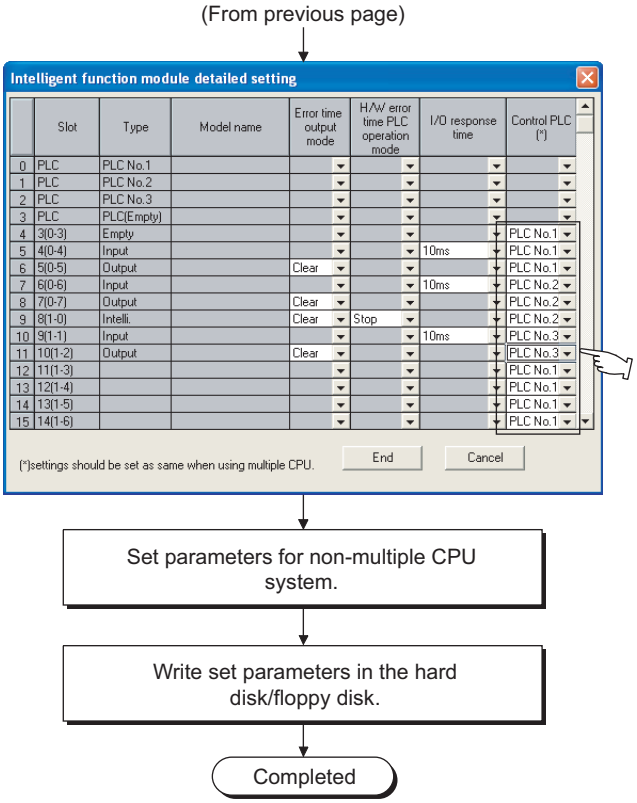


Select "I/O assignment" and display the I/O assignment setting window.



Check the I/O assignment settings and basic settings in the I/O assignment setting window. Select "Detailed setting" and display the detail setting window.

(To next page)



Check settings of the control CPU.

Diagram 8.5 Parameter setting procedure for reusing multiple CPU system parameters

8.2.2 Parameter setting for the Universal model QCPU

(1) System configuration

Diagram 8.2 shows an example procedures for setting up the multiple CPU system parameters.

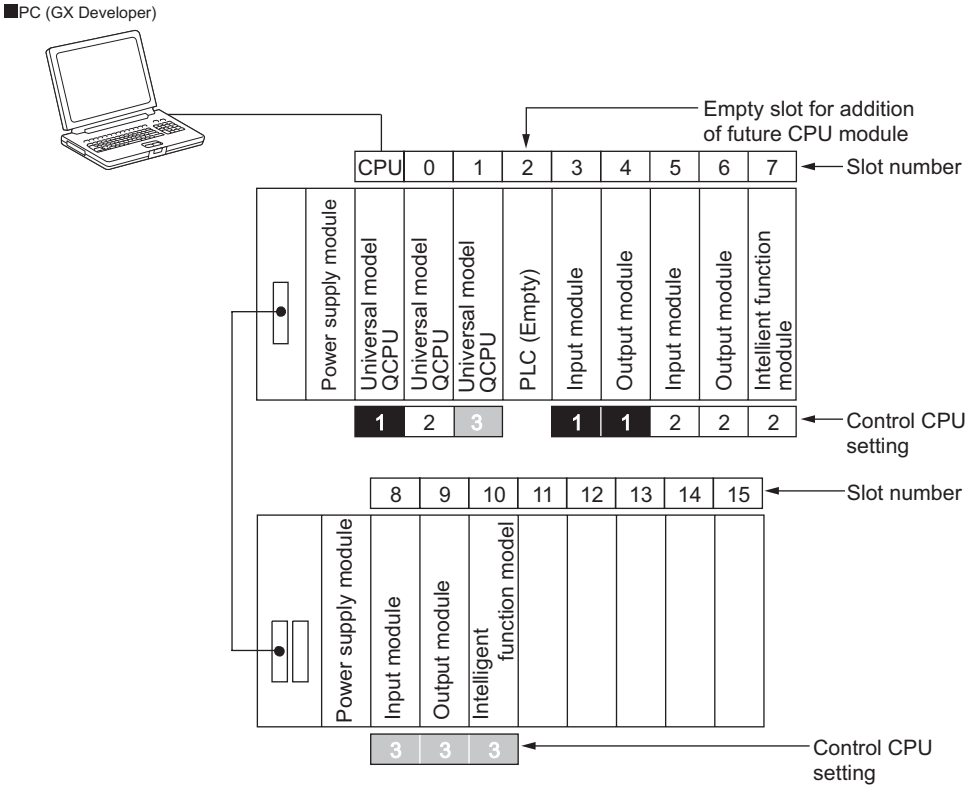


Diagram 8.6 Configuration example of multiple CPU system

(2) Parameters required for multiple CPU system

When the multiple CPU system is used, the following parameter settings are required. Parameters of "Same setting items for each CPU module" should be set with the same settings in all CPU modules used in the multiple CPU system except some parts.(☞ Section 6.1)

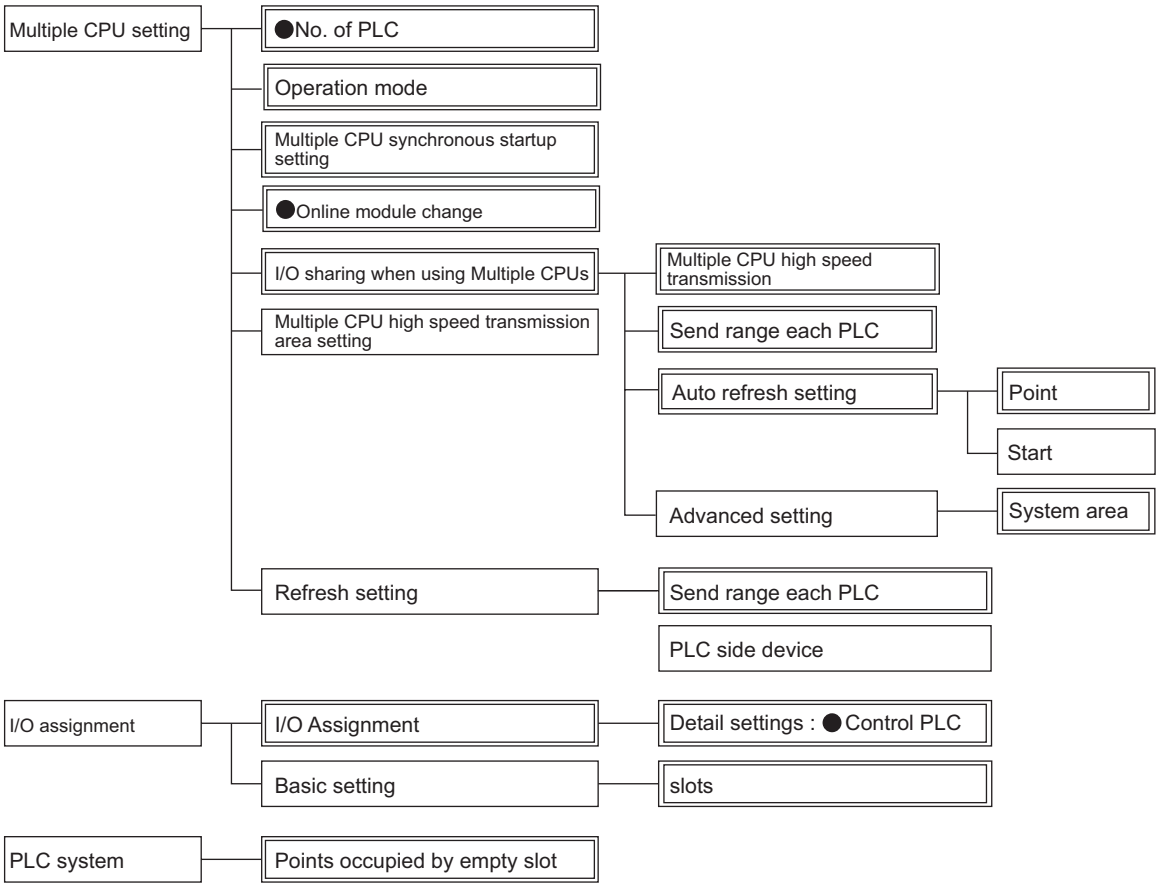
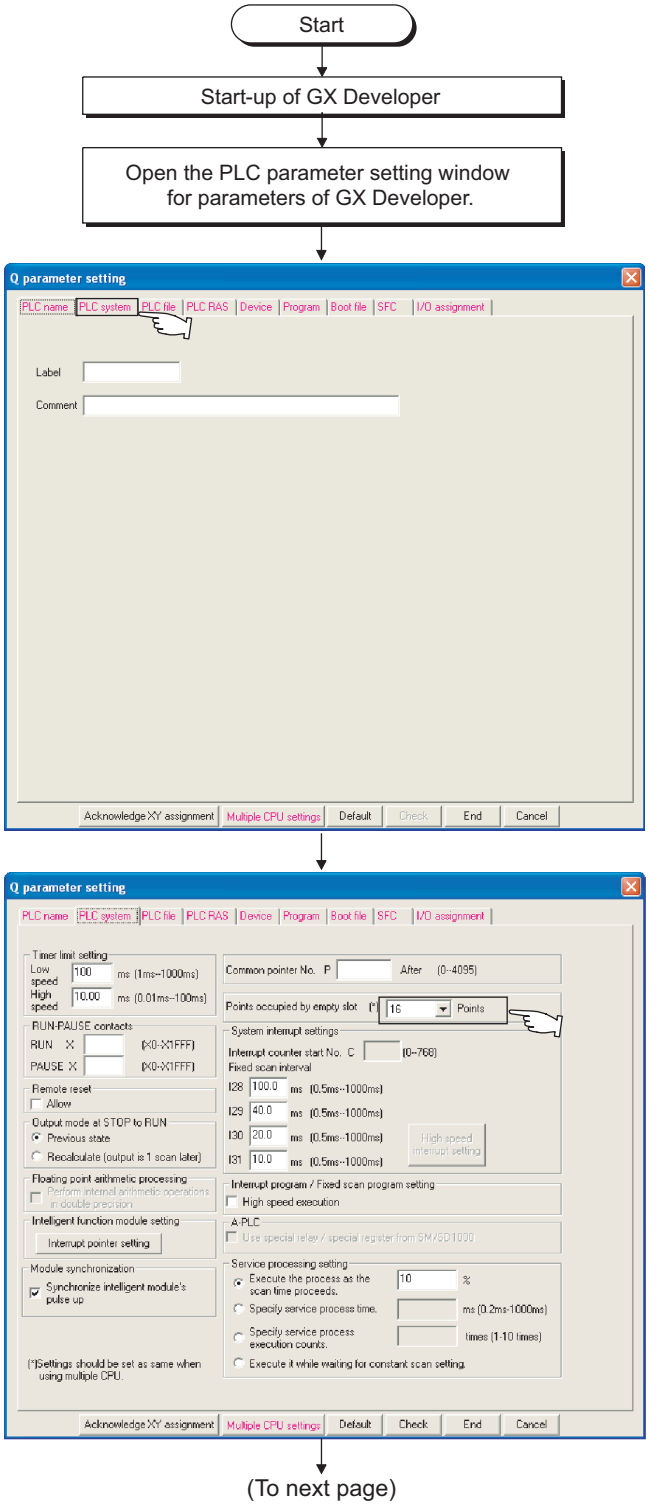


Diagram 8.7 List of parameters required for multiple CPU system

(3) When creating a new multiple CPU system



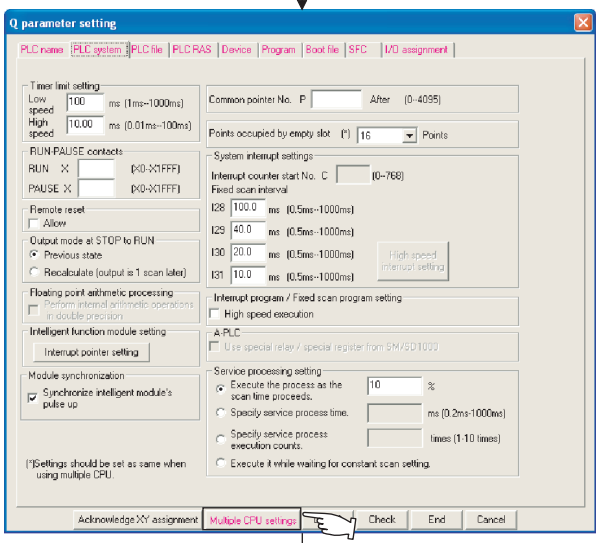
☞ The operating manual of GX Developer.

☞ The operating manual of GX Developer.

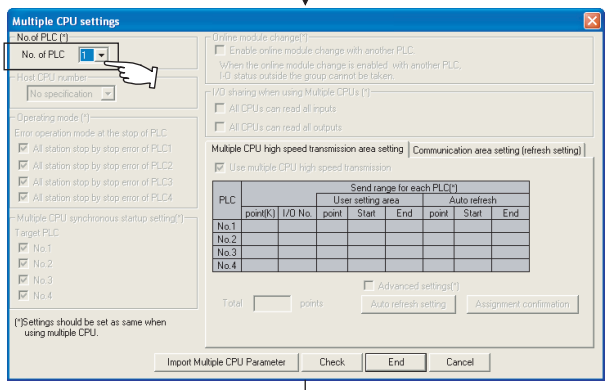
Select "PLC system" and display the PLC system setting window.

Points occupied by empty slot (Option)
· Set the occupied points for one empty slot.
Default: 16 points

(From previous page)

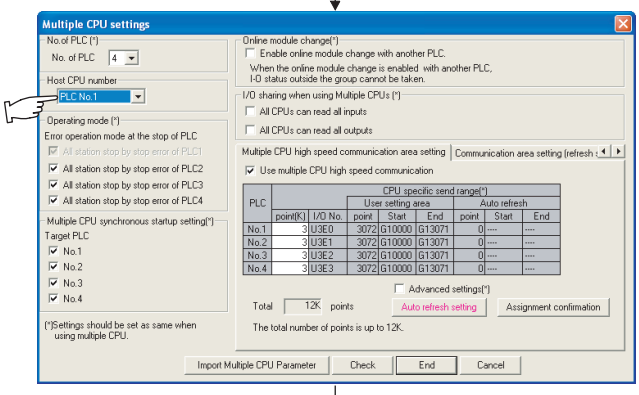


Select "Multiple CPU settings" and display the multiple CPU setting window.



No. of PLC (mandatory item)

· Set the number of CPU modules mounted on the main base unit with the multiple CPU system.



Host CPU number

· Setting is required when checking the host CPU number of the multiple CPU system. (Refer to Section 3.11)
Default: No specification

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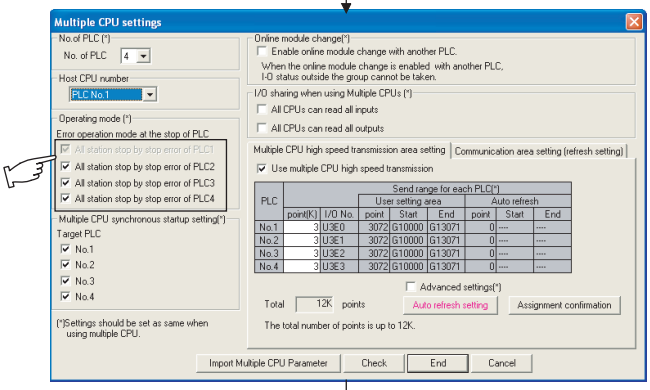
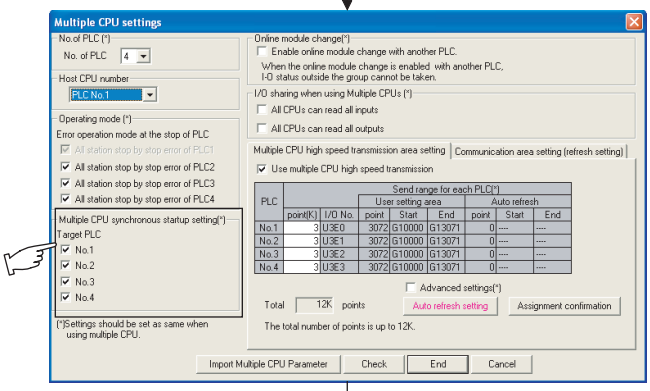


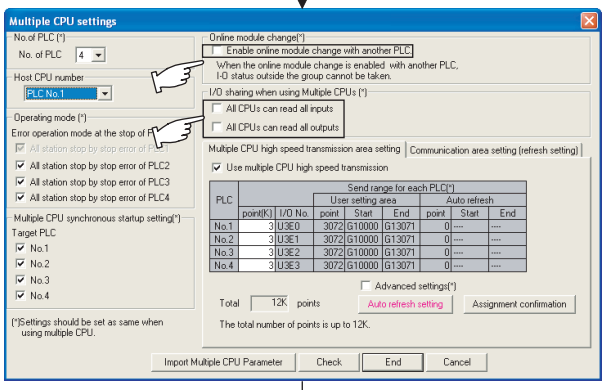
Operating mode (option)

- Select if all CPUs are stopped/operated for occurrence of stop error.
  Default: With any error of CPUs 2, 3 and 4, all CPUs stop (checked).
- For example, when "All station stop by stop error of PLC 2" is unchecked, other CPUs continue operation for an error of CPU No. 2.
- Operation of CPU No. 1 cannot be changed.



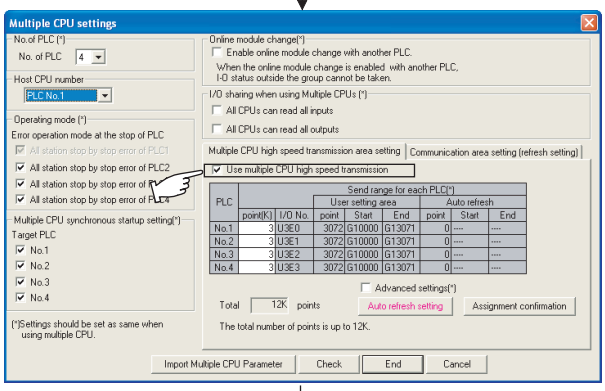
Multiple CPU synchronized boot-up setting

- Select whether to start CPU modules simultaneously in a multiple CPU system.
  Default: All CPUs synchronized boot-up (Checked)



I/O sharing when using Multiple CPUs (Option)

- Set if the input/output status beyond control of input/output setting outside of group is loaded or not.
  Default: Not loaded. (Not checked)



Multiple CPU high speed transmission

- Select whether to use the multiple CPU high speed transmission function or not (Refer to Section 4.5)
  Default: Selected to use the multiple CPU high speed transmission function

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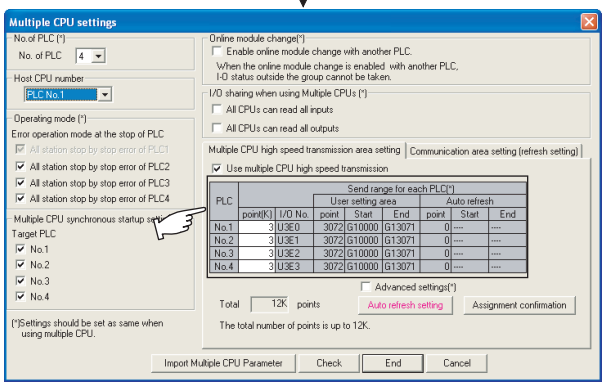
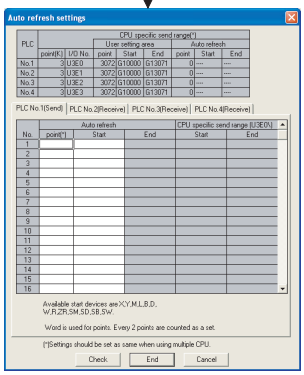


The number of points setting in Send range for each PLC

- Set the number of points to be sent/received among CPU modules.
- Set them within the following number of points.

No. of PLC	Setting range
2	0 to 14k points
3	0 to 13k points
4	0 to 12k points

- Set 0 point for the following CPU modules:
  High Performance model QCPU
  Process CPU
  PC CPU module

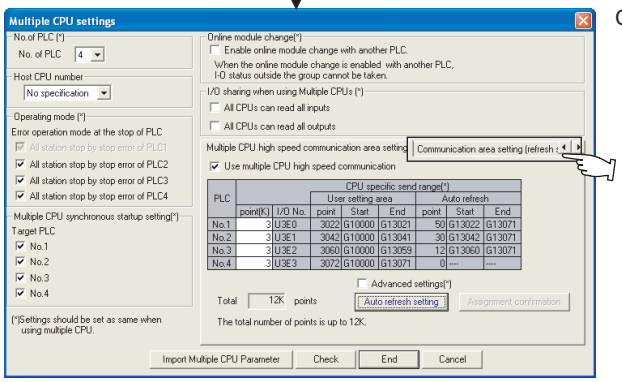


Auto refresh setting (Option)

- Set devices and the number of points for data communication with auto refresh among CPU modules.
- The number of points in the table below is occupied with one point in the auto refresh area.

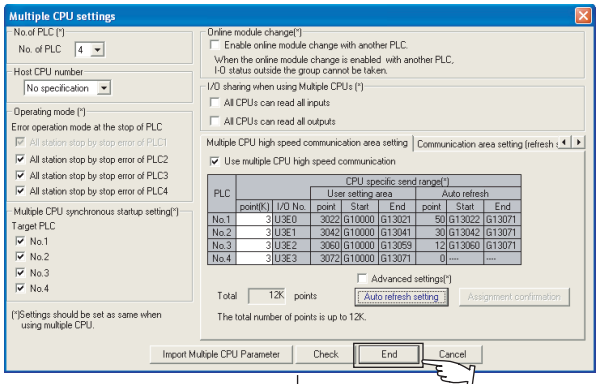
Device	Occupied points
X,Y,M,L,B,SM,SB	16 points
D,W,R,ZR,SD,SW	1 point

- Set them by the number of CPUs (Selection among CPU No.1 to CPU No.4) set on the Multiple CPU settings.
  After the settings, select the "End" button to close the Auto refresh settings window.



Communication area setting (refresh setting)

- Setting is required when performing communication with the following CPU modules.
  - High Performance model QCPU
  - Process CPU
  - PC CPU module



- After setting, select "Setting completed" and close the multiple CPU setting window.

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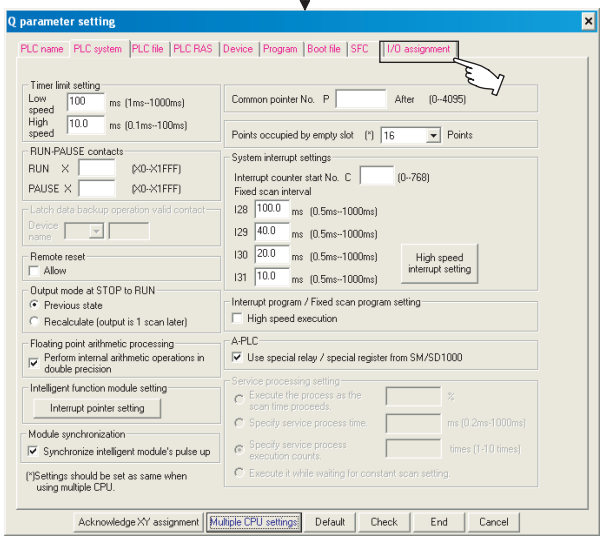
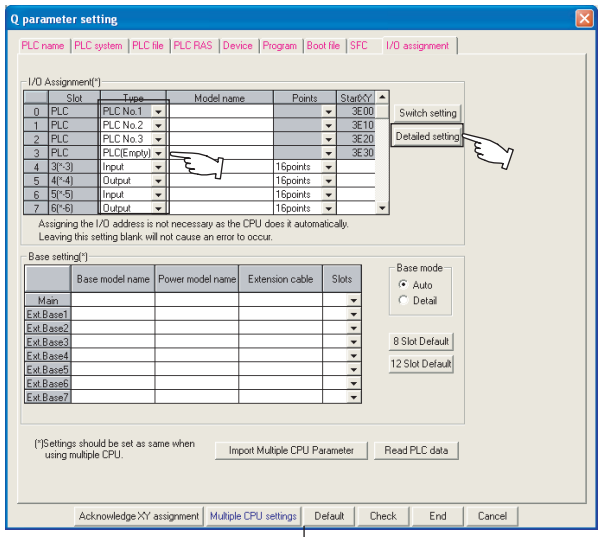


Select "I/O assignment" and display the I/O assignment setting window.



I/O assignment (option)

- Select the slot to "PLC (empty)" that does not mount the CPU module for each type.
- Select the type of each module from the pulldown menu.
- Select "Detailed setting" on the I/O assignment setting window and display the detail setting window.

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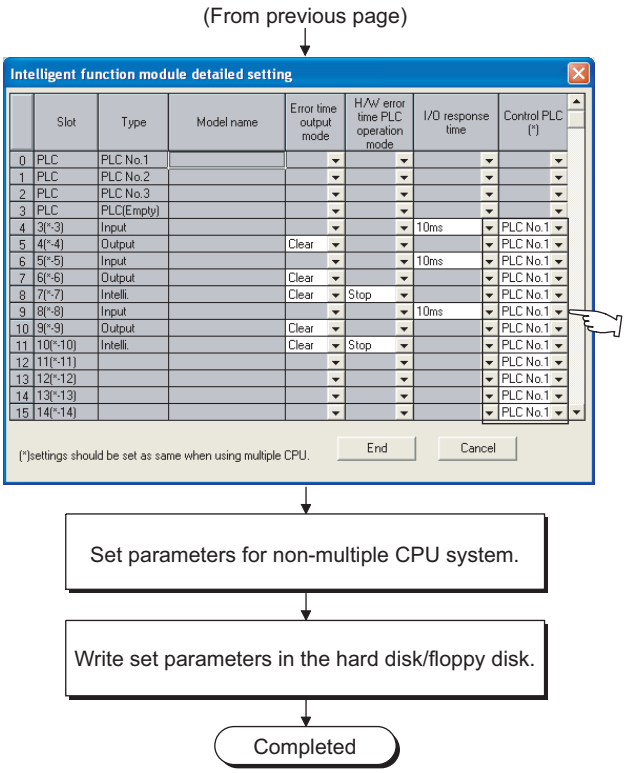
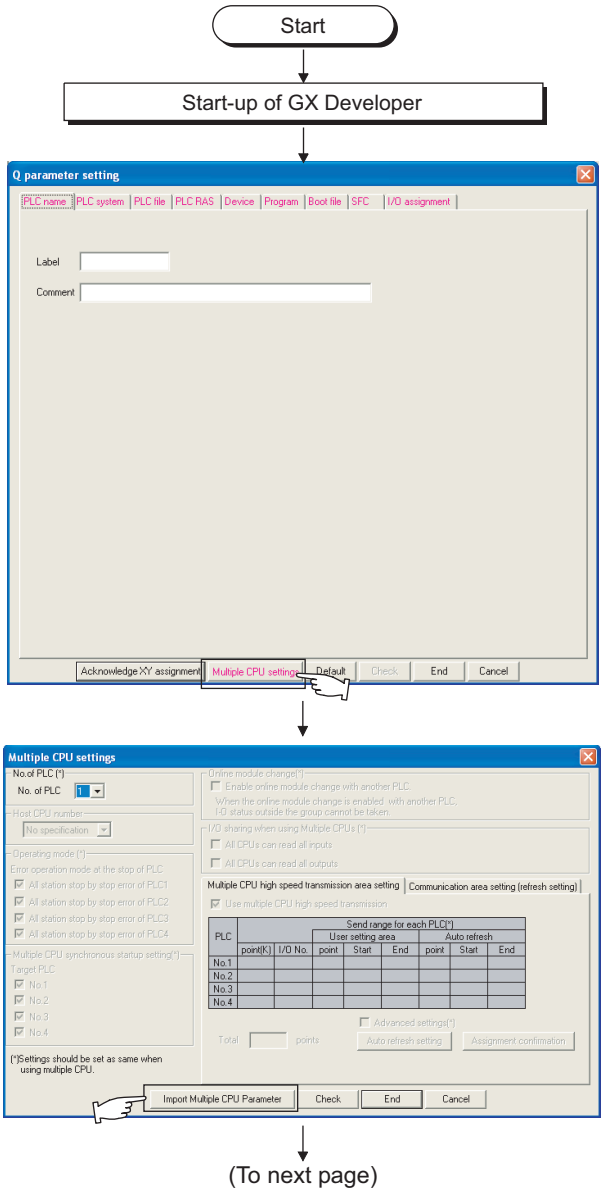


Control PLC (mandatory item)
· Select control CPU (PLC No. 1 to PLC No. 4) for each slot.

Diagram 8.8 Parameter setting procedure for new multiple CPU system creation

8.2.3 Reusing preset multiple CPU parameters



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☞Refer to the operating manual of GX Developer.

Open the PLC parameter setting window for the parameter of GX Developer.
Select "Multiple CPU settings" and display the multiple CPU setting window.

Carry-over of multiple CPU setting
· Click "Import Multiple CPU Parameter".

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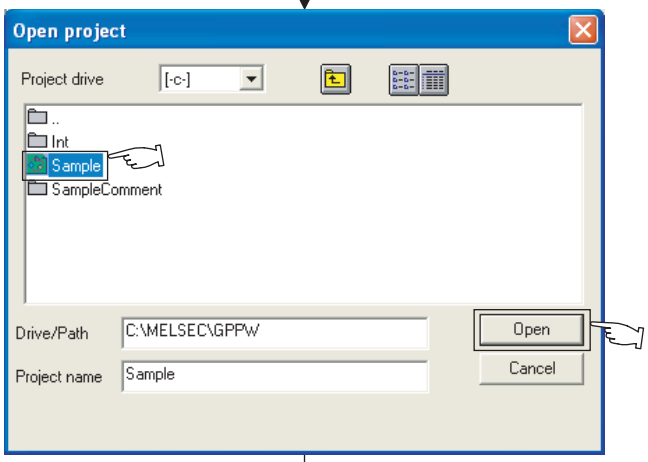
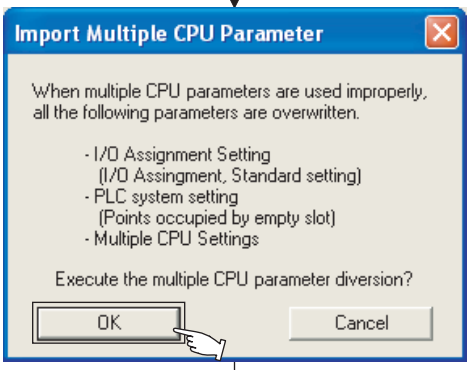
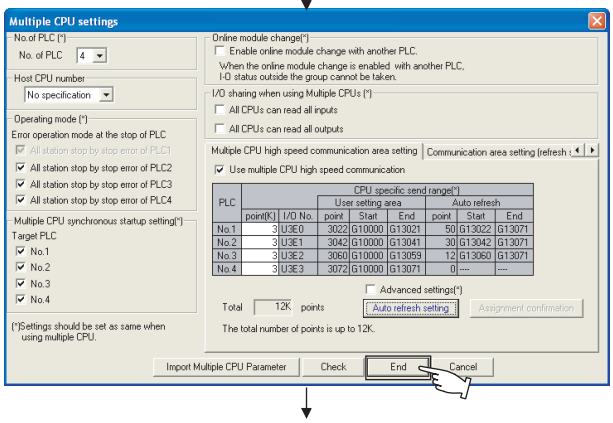


Setting of carry-over project
- Select the project that carries over multiple CPU setting and I/O assignment.
- Click "Open".



When "OK" is selected, the multiple CPU setting and the I/O assignment setting data are read from the specified project and the data is overwritten.



Check the multiple CPU settings.
When changing a device in auto refresh setting, select "Auto refresh" and input a device number to be changed.
(Items with * should have the same settings for each CPU module.)

After checking the multiple CPU settings or completion of correction, select "END" and close the multiple CPU setting window.

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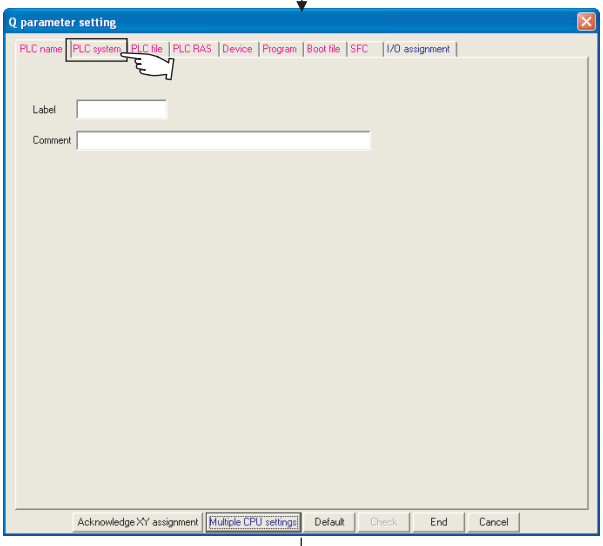
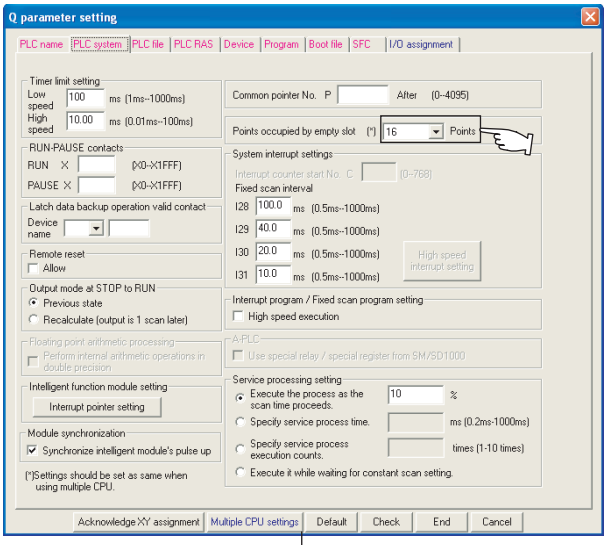


Select "PLC system" and display the PLC system setting window.



Check the empty slot points on the PLC system setting window.

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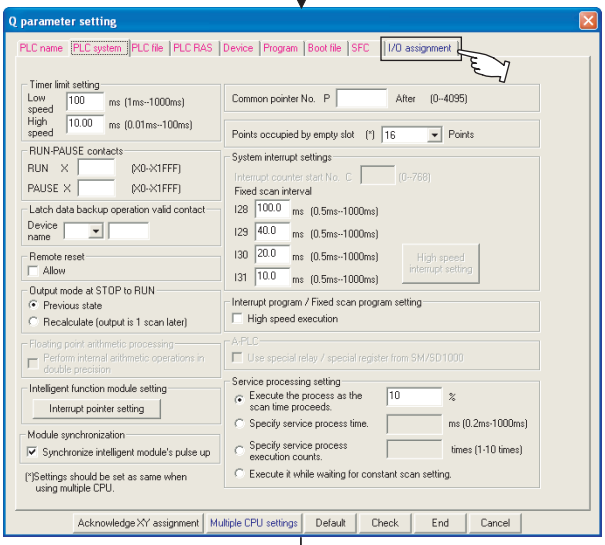
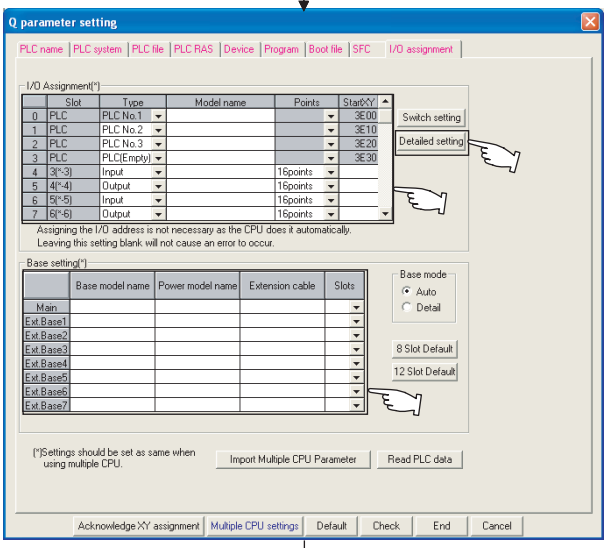
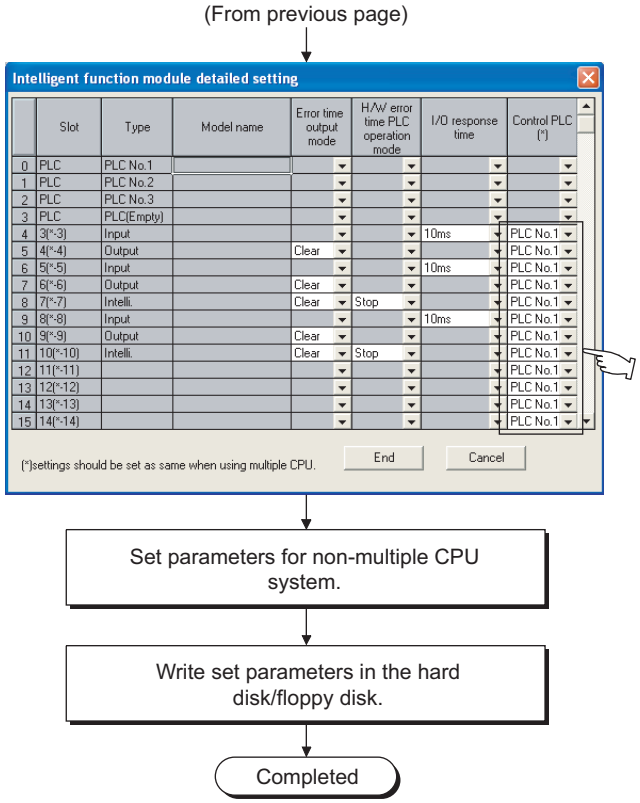


Select "I/O assignment" and display the I/O assignment setting window.



Check the I/O assignment settings and basic settings in the I/O assignment setting window. Select "Detailed setting" and display the detail setting window.

(To next page)



Check settings of the control CPU.

Diagram 8.9 Parameter setting procedure for reusing multiple CPU system parameters

8.3 Communication program example using auto refresh

This section explains a program example in the following system configuration given in Diagram 8.10 and assignment of the data communications between CPU modules.

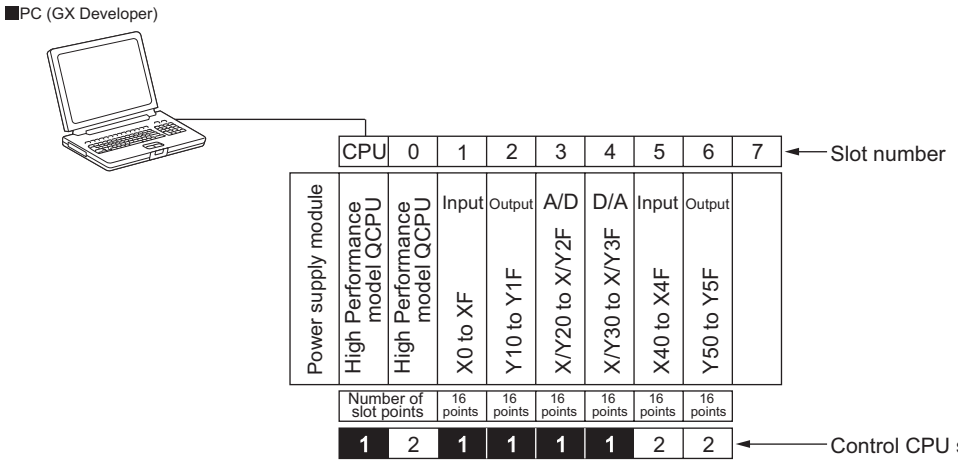


Diagram 8.10 Configuration example of multiple CPU system

8.3.1 Program example for the Basic model QCPU High Performance model QCPU and Process CPU

(1) I/O assignment and auto refresh settings

I/O assignment of each module and setting example of the auto refresh area are shown in Diagram 8.11.

For the I/O assignment settings, refer to Section 3.3.

For the auto refresh area settings, refer to Section 4.1.4)

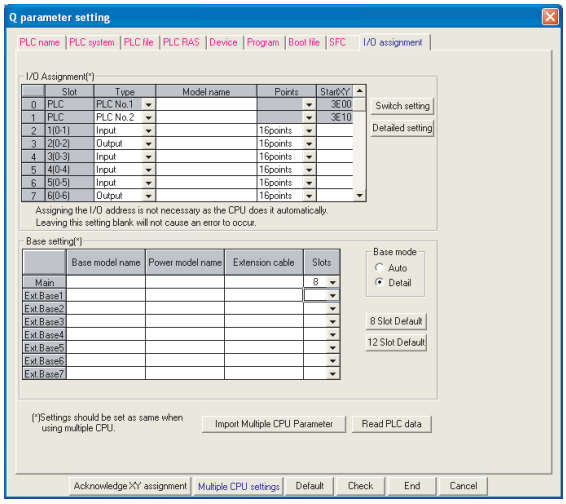


Diagram 8.11 I/O assignment settings of each module

Change screens: Setting 1 ☐ Set starting devices for each PLC

PLC	Send range for each PLC (The auto refresh area Caution)			PLC side device	
	Point (*)	Start	End	Dev. starting	D0
				Start	End
No.1	32	0000	001F	D0	D31
No.2	32	0000	001F	D32	D63
No.3					
No.4					

Change screens: Setting 2 ☐ Set starting devices for each PLC

PLC	Send range for each PLC (The auto refresh area Caution)			PLC side device	
	Point (*)	Start	End	Dev. starting	M0
				Start	End
No.1	2	0020	0021	M0	M31
No.2	2	0020	0021	M32	M63
No.3					
No.4					

Diagram 8.12 Auto refresh area settings

(2) Example of bit & word data transmission from CPU No. 1 to No. 2

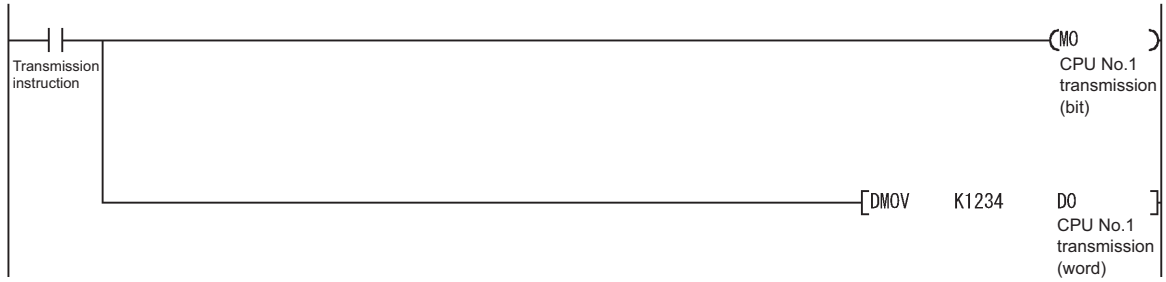
Table8.1 Auto refresh devices used in each CPU module

Auto refresh devices used in CPU No. 1	Auto refresh devices used in CPU No. 2
M0	M0
D0,D1	D0,D1

Program example

Program by which bit and word data are sent from CPU No. 1 to CPU No. 2

CPU No. 1



CPU No. 2

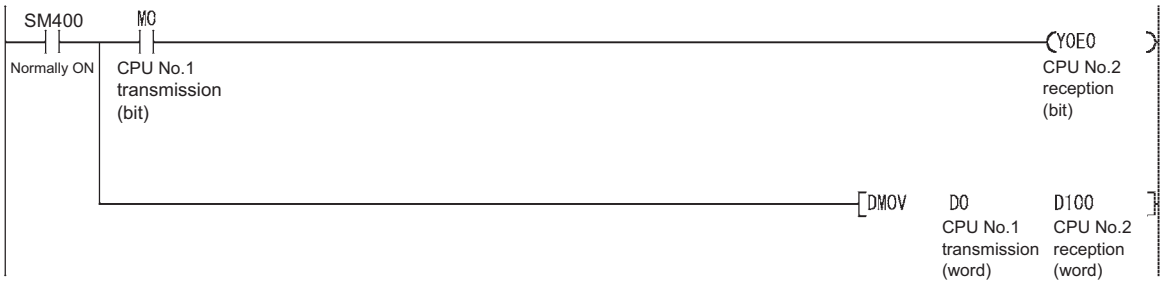


Diagram 8.13 Program example for sending bit and word data from CPU No. 1 to CPU No. 2

(3) Example of continuous data transmission from CPU No. 1 to No. 2

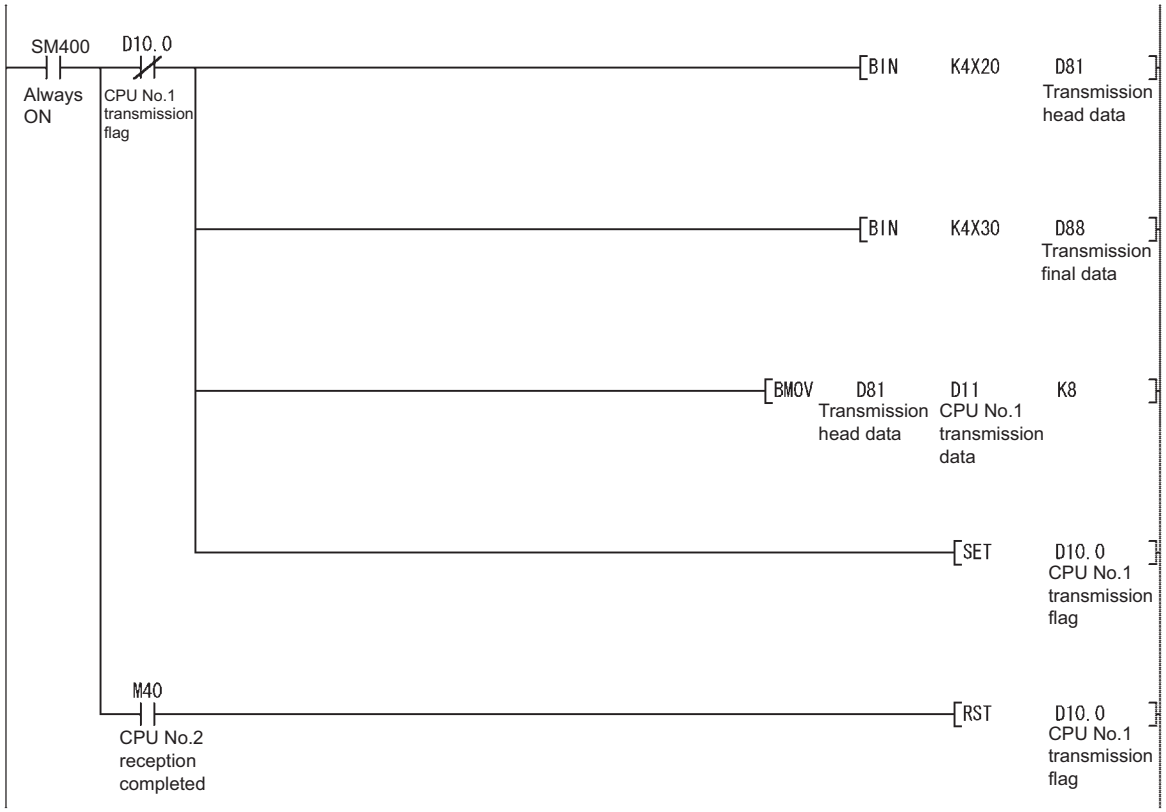
Table8.2 Auto refresh devices used in each module

Auto refresh devices used in CPU No. 1	Auto refresh devices used in CPU No. 2
D10 to D18	D10 to D18 M40

For handshake in CPU Nos. 1 and 2, refer to Section 4.1.2.

Program example
Program by which data are continuously stored from CPU No. 1 to CPU No. 2

CPU No. 1



CPU No. 2

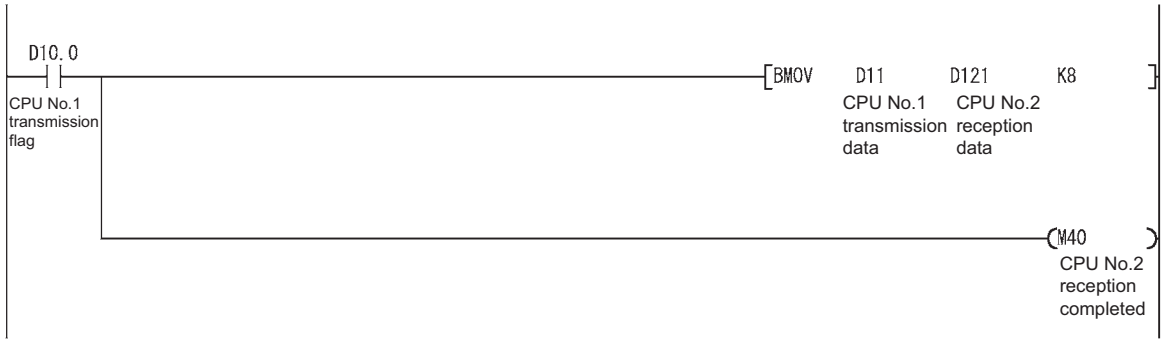


Diagram 8.14 Program example for storing data continuously from CPU No. 1 to CPU No. 2

(4) Write/read using user setting area of shared memory by program

(a) Memory addresses for auto refresh setting to user setting area

In the auto refresh setting, make same settings for CPU No. 1 and CPU No. 2.

Change screens: Setting 1 — Set starting devices for each PLC

PLC	Send range for each PLC			PLC side device	
	The auto refresh area Caution)			Dev. starting	D0
	Point (*)	Start	End	Start	End
No.1	32	0000	001F	D0	D31
No.2	32	0000	001F	D32	D63
No.3					
No.4					

Change screens: Setting 2 — Set starting devices for each PLC

PLC	Send range for each PLC			PLC side device	
	The auto refresh area Caution)			Dev. starting	M0
	Point (*)	Start	End	Start	End
No.1	2	0020	0021	M0	M31
No.2	2	0020	0021	M32	M63
No.3					
No.4					

Diagram 8.15 Auto refresh setting (same settings)

The auto refresh area occupies the area from setting 1 and setting 2 to memory address of 0800H to 0821H.
Therefore, the user setting area is in a range from 0822H to 0FFFH.
(☞ Section 4.1.1)

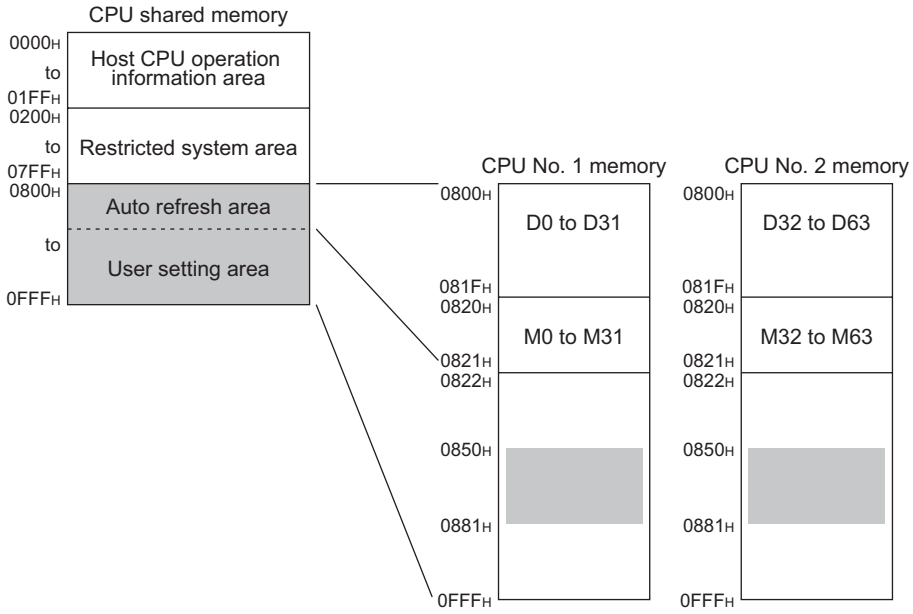


Diagram 8.16 Range of auto refresh area and user setting area

(b) Program example of continuous data writing/reading using the user setting area from CPU No. 2 to CPU No. 1

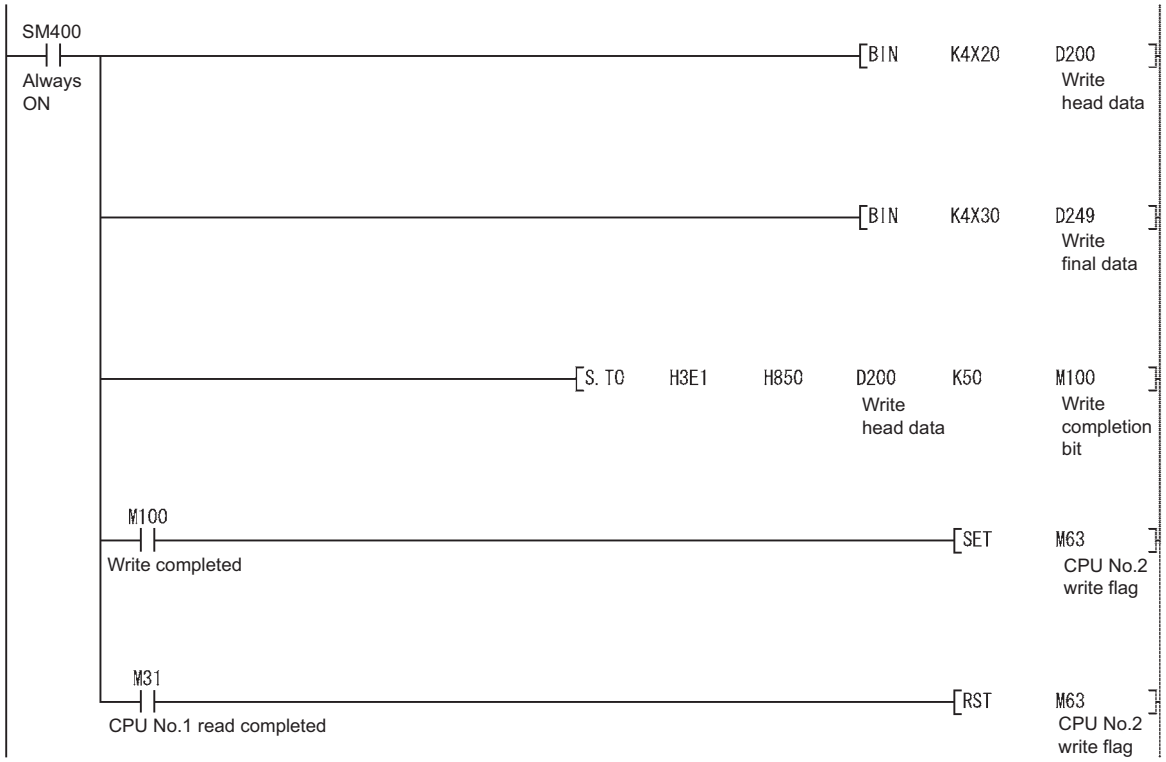
Table8.3 Auto refresh devices used in each CPU module

Auto refresh device used in CPU No. 2	Auto refresh device used in CPU No. 1
M63	M31

Program example

Program by which data are continuously written/read using the user setting area from the CPU module of CPU No. 2 to the CPU module of CPU No. 1.

CPU No. 2



CPU No. 1

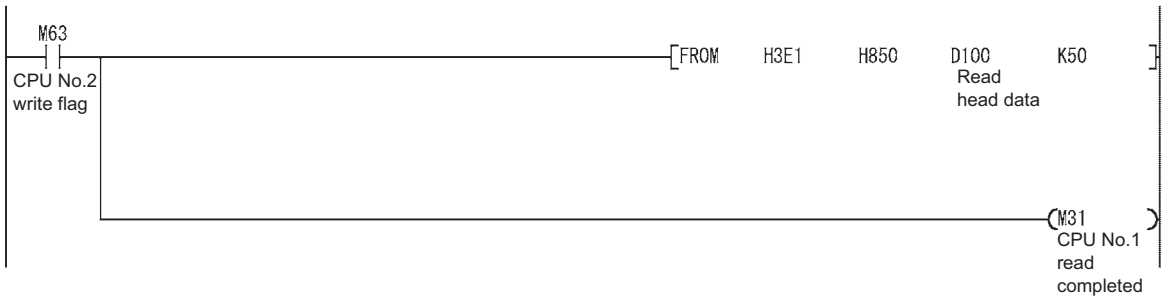


Diagram 8.17 Program example for continuously writing/reading data using the user setting area from CPU No. 2 to CPU No. 1

8.3.2 Program example for the Universal model QCPU

This section explains a program example in the following system configuration given in Diagram 8.10 and assignment of the data communications between CPU modules.

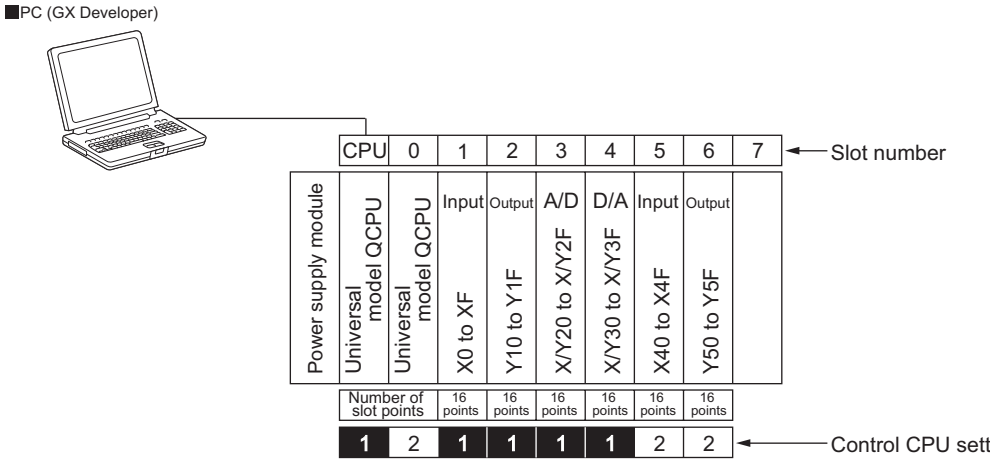


Diagram 8.18 Configuration example of multiple CPU system

(1) I/O assignment and auto refresh settings

I/O assignment of each module and setting example of the auto refresh area are shown in Diagram 8.11.

For the I/O assignment settings, refer to Section 3.3.

For the auto refresh area settings, refer to Section 4.1.4)

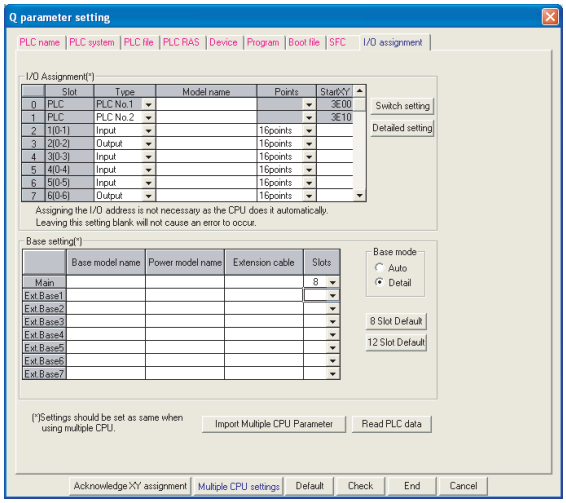


Diagram 8.19 I/O assignment settings of each module

Setting of CPU No.1

PLC No.1 | PLC No.2

No.	Auto refresh			Send range for each PLC (U3E0\)	
	point(*)	Start	End	Start	End
1	2	M0	M31	G17134	G17135
2	32	D0	D31	G17136	G17167
3					
4					
5					
6					

PLC No.1 | PLC No.2

No.	Auto refresh			Send range for each PLC (U3E1\)	
	point(*)	Start	End	Start	End
1	2	M32	M63	G17134	G17135
2	32	D32	D63	G17136	G17167
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					

The applicable devices of start device are X,Y,M,L,B,D,W,R,ZR,SM,SD,SB,SW.

The unit of the point is word.

Setting of CPU No.2

PLC No.1 | PLC No.2

No.	Auto refresh			Send range for each PLC (U3E0\)	
	point(*)	Start	End	Start	End
1	2	M0	M31	G17134	G17135
2	32	D0	D31	G17136	G17167
3					
4					
5					
6					

PLC No.1 | PLC No.2

No.	Auto refresh			Send range for each PLC (U3E1\)	
	point(*)	Start	End	Start	End
1	2	M32	M63	G17134	G17135
2	32	D32	D63	G17136	G17167
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					

The applicable devices of start device are X,Y,M,L,B,D,W,R,ZR,SM,SD,SB,SW.

The unit of the point is word.

Diagram 8.20 Auto refresh area setting

(2) Example of bit & word data transmission from CPU No. 1 to No. 2

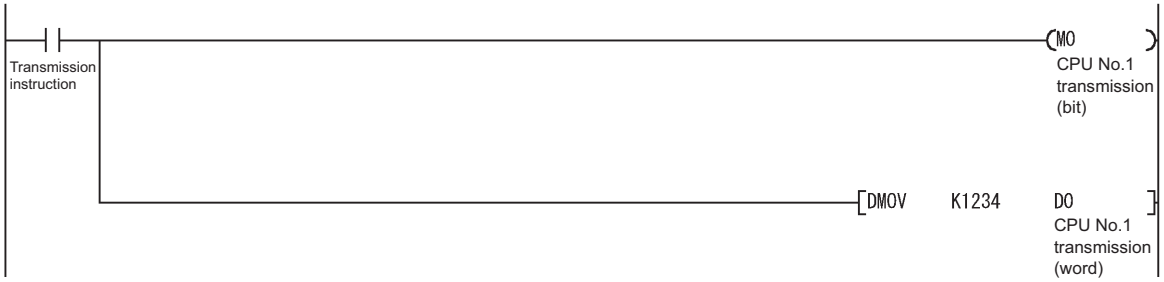
Table8.4 Auto refresh devices used in each CPU module

Auto refresh devices used in CPU No. 1	Auto refresh devices used in CPU No. 2
M0	M0
D0,D1	D0,D1

Program example

Program by which bit and word data are sent from CPU No. 1 to CPU No. 2

CPU No. 1



CPU No. 2

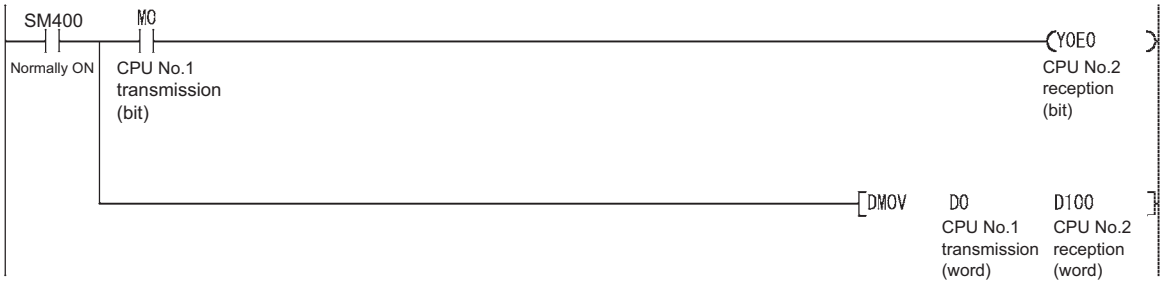


Diagram 8.21 Program example for sending bit and word data from CPU No. 1 to CPU No. 2

(3) Example of continuous data transmission from CPU No. 1 to No. 2

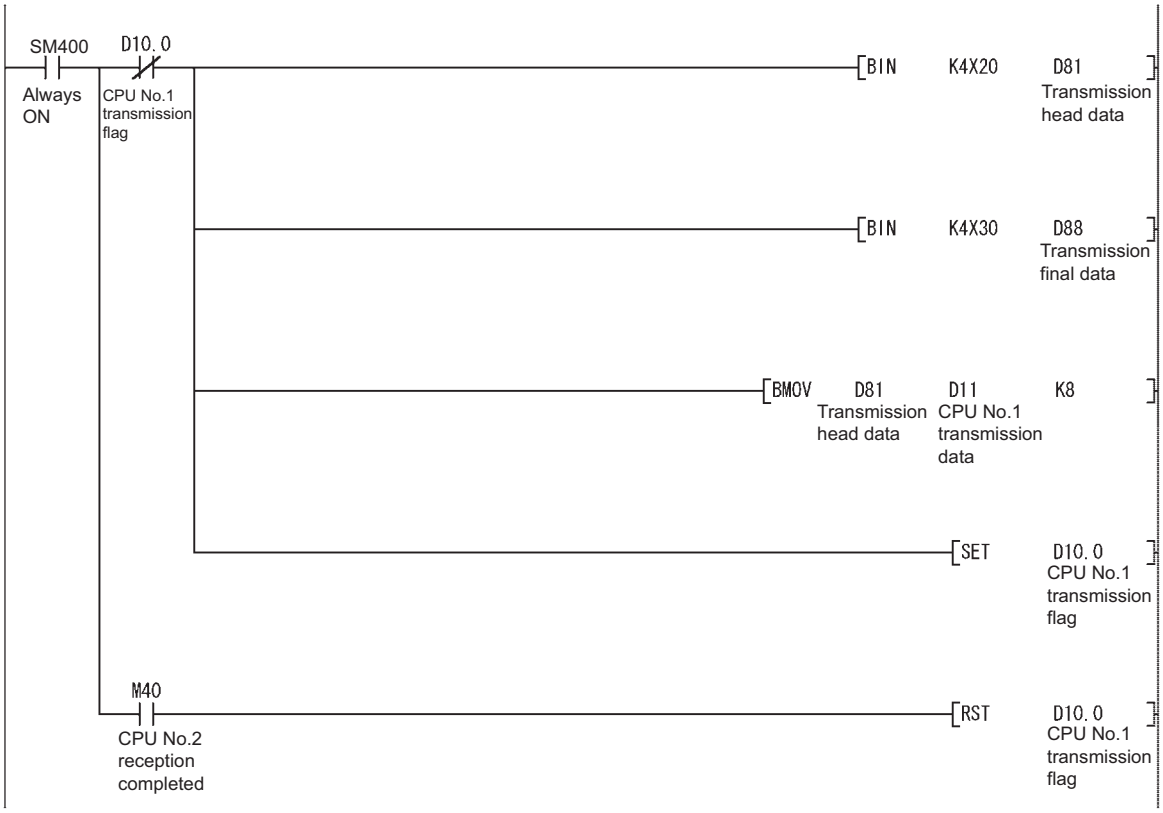
Table8.5 Auto refresh devices used in each module

Auto refresh devices used in CPU No. 1	Auto refresh devices used in CPU No. 2
D10 to D18	D10 to D18 M40

For handshake in CPU Nos. 1 and 2, refer to Section 4.1.2.

Program example
Program by which data are continuously stored from CPU No. 1 to CPU No. 2

CPU No. 1



CPU No. 2

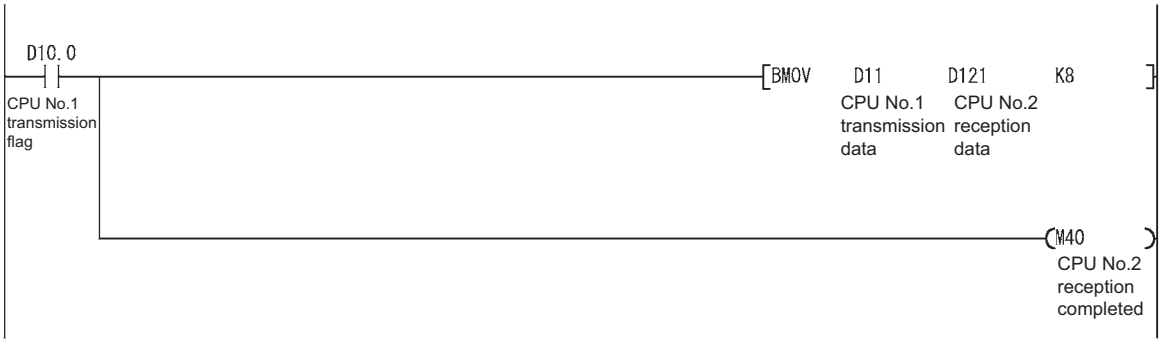


Diagram 8.22 Program example for storing data continuously from CPU No. 1 to CPU No. 2

(4) Write/read using user setting area of shared memory by program

(a) Memory addresses for auto refresh setting to user setting area

In the auto refresh setting, make same settings for CPU No. 1 and CPU No. 2.

Setting of CPU No.1

PLC No.1 | PLC No.2

No.	Auto refresh point(*)	Auto refresh Start	Auto refresh End	Send range for each PLC (U3E0\) Start	Send range for each PLC (U3E0\) End
1	2	M0	M31	G17134	G17135
2	32	D0	D31	G17136	G17167
3					
4					
5					
6					

PLC No.1 | PLC No.2

No.	Auto refresh point(*)	Auto refresh Start	Auto refresh End	Send range for each PLC (U3E1\) Start	Send range for each PLC (U3E1\) End
1	2	M32	M63	G17134	G17135
2	32	D32	D63	G17136	G17167
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					

The applicable devices of start device are X,Y,M,L,B,D,W,R,ZR,SM,SD,SB,SW.

The unit of the point is word.

Setting of CPU No.2

PLC No.1 | PLC No.2

No.	Auto refresh point(*)	Auto refresh Start	Auto refresh End	Send range for each PLC (U3E0\) Start	Send range for each PLC (U3E0\) End
1	2	M0	M31	G17134	G17135
2	32	D0	D31	G17136	G17167
3					
4					
5					
6					

PLC No.1 | PLC No.2

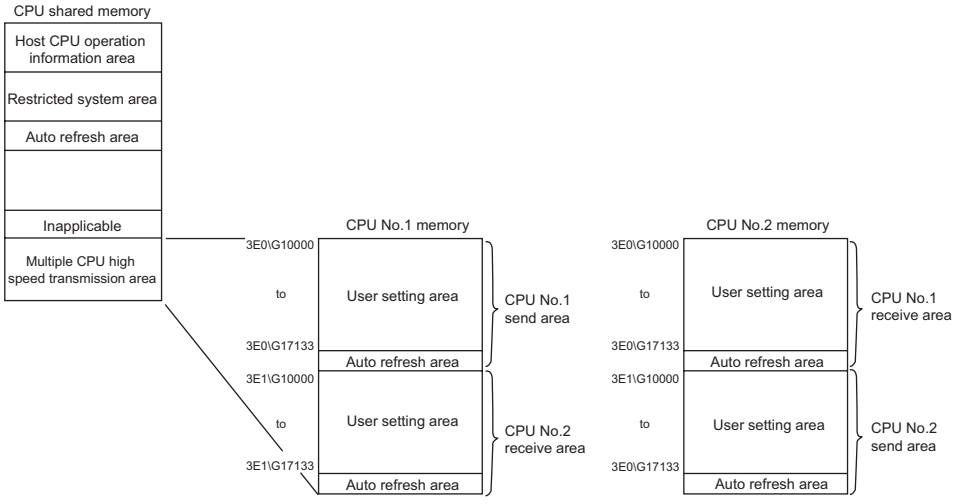
No.	Auto refresh point(*)	Auto refresh Start	Auto refresh End	Send range for each PLC (U3E1\) Start	Send range for each PLC (U3E1\) End
1	2	M32	M63	G17134	G17135
2	32	D32	D63	G17136	G17167
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					

The applicable devices of start device are X,Y,M,L,B,D,W,R,ZR,SM,SD,SB,SW.

The unit of the point is word.

Diagram 8.23 Auto refresh setting (same settings)

User free area will be from 3E0\G10000 for CPU No.1 and from 3E1\G10000 for CPU No.2.



(5) Program example of continuous data writing/reading using the user setting area from CPU No. 2 to CPU No. 1

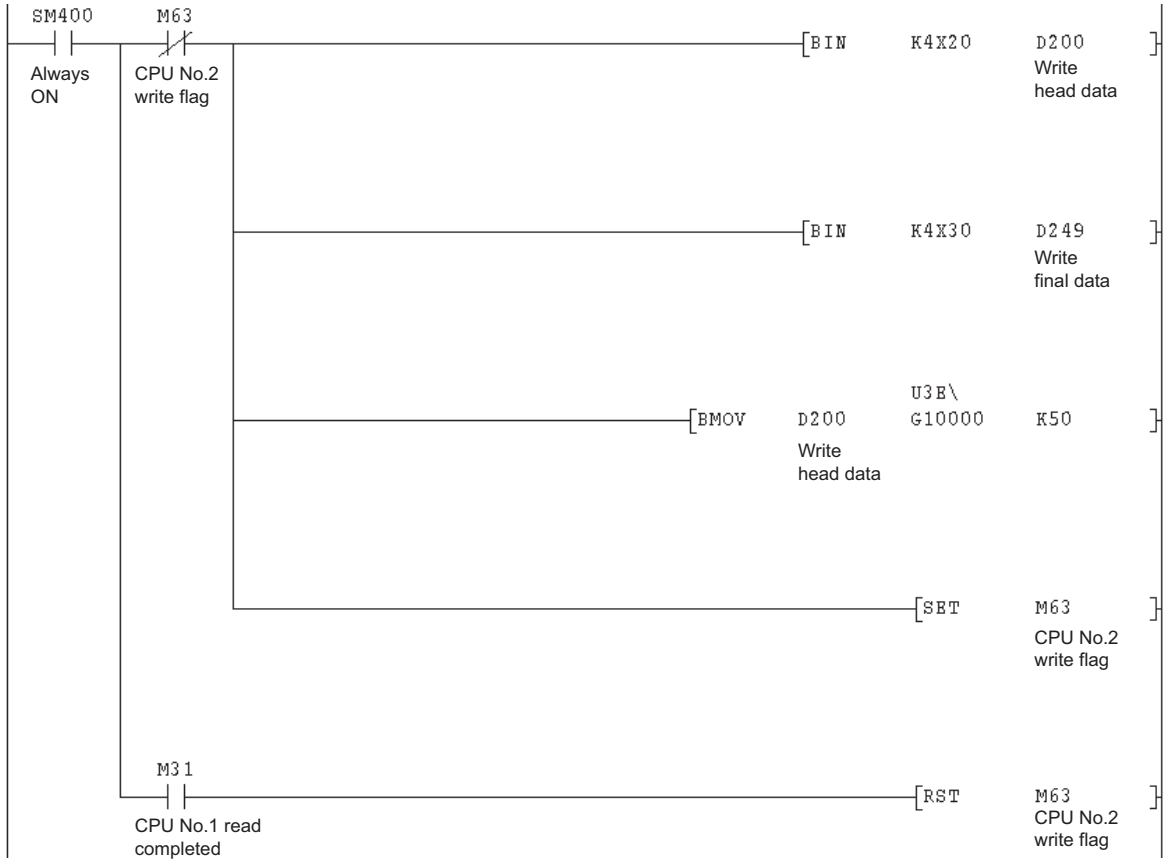
Table8.6 Auto refresh devices used in each CPU module

Auto refresh device used in CPU No. 2	Auto refresh device used in CPU No. 1
M63	M31

Program example

Program by which data are continuously written/read using the user setting area from the CPU module of CPU No. 2 to the CPU module of CPU No. 1.

CPU No. 2



CPU No. 1

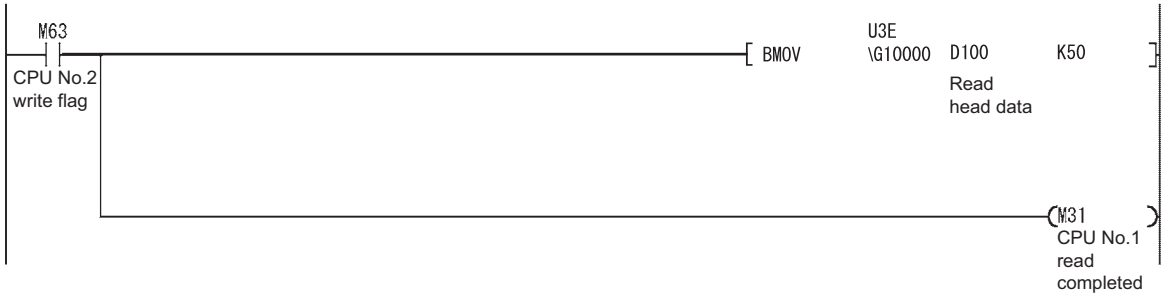


Diagram 8.24 Program example for continuously writing/reading data using the user setting area from CPU No. 2 to CPU No. 1

APPENDICES

Appendix 1 Transportation Precautions

When transporting lithium batteries, make sure to treat them based on the transport regulations.

Appendix 1.1 Controlled models

The batteries for the QCPU (including memory cards) are classified as follows:

TableApp.1 List of models for restricted transportation

Product name	Model	Product supply status	Classification for transportation
Battery	Q8BAT	Lithium battery (assembled battery)	Dangerous goods
Battery	Q8BAT-SET	Lithium battery (assembled battery) + Q8BAT connection cable	
Battery	Q7BAT	Lithium battery	
Battery	Q7BAT-SET	Lithium battery with holder	
Battery	Q6BAT	Lithium battery	Non-dangerous goods
Memory card battery	Q2MEM-BAT	Lithium coin battery	
Memory card	Q2MEM-1MBS Q2MEM-2MBS	Packed with lithium coin battery (Q2MEM-BAT)	
	Q3MEM-4MBS Q3MEM-8MBS	Packed with lithium coin battery (Q3MEM-BAT)	
	Q3MEM-4MBS-SET Q3MEM-8MBS-SET	Packed with lithium coin battery (Q3MEM-BAT) + Memory card protective cover	

Appendix 1.2 Transport guidelines

Comply with IATA Dangerous Goods Regulations, IMDG code and the local transport regulations when transporting products after unpacking or repacking, while Mitsubishi ships products with packages to comply with the transport regulations.
Also, contact the transporters.

Memo

INDEX

[A]

A series. A-19
A series power supply module A-20
Access range of GX Developer 3-25
Access with instruction using link direct device . 3-24
AnS series A-19
AnS series power supply module A-20
Auto refresh 4-9
Auto refresh area 4-3,4-7
Auto refresh setting 4-11,6-8

[B]

Base unit
  Extension base unit. A-20
  Main base unit. A-20
  Redundant base unit. A-20
  Redundant extension base unit. A-20
  Redundant main base unit A-20
  Slim type main base unit. A-20
Basic model QCPU. A-19

[C]

Communication between multiple CPUs with dedicated instructions. 4-51
Communication using CPU shared memory by program 4-38
Communication with instructions dedicated to communication 4-51
Communication with motion CPU. 4-49,4-51
Communication with PC CPU module 4-53
Communications with instructions dedicated to motion CPU 4-2,4-49
Consistency check between CPU modules 6-5
Control CPU A-21
Control CPU settings 6-9
Controlled module A-21
CPU shared memory 4-3
  Auto refresh using CPU shared memory 4-8
  Communication using CPU shared memory by program. 4-38

[E]

Extension base unit A-20

[F]

Factors for prolonged scan time 5-3
Flow-chart
  Flow-chart for starting up the multiple CPU system 8-1
  Reusing preset multiple CPU settings and I/O assignment 8-10,8-23
  When creating a new multiple CPU system 8-5,8-17
Function version 2-42

[G]

GOT A-21
GX Configurator 2-47
GX Developer A-19,2-46

[H]

High Performance model QCPU. A-19
Host CPU operation information area. 4-3,4-6

[I]

I/O number assignment 3-14
I/O settings outside of the group. 3-17,6-8
Instructions dedicated to communication between multiple CPUs 4-51
Instructions dedicated to motion CPU 4-49
Intelligent function module device. 4-39

[L]

Link direct device 3-24

[M]

Main base unit A-20
Maximum number of extension units 2-4,2-8
Mounting position 3-1
Multiple CPU settings 6-1

[N]

Network modules 2-49
No. of CPU setting 6-6
Non-control CPU. A-21
Non-controlled module A-21
Note6.2 6-2

[O]

Online module change 2-45
Online module change setting 6-8
Operating mode at stop error 3-30,6-8
Operating mode setting 6-8
Operation for CPU module stop error 3-30

[P]

Parameter setting 6-1
Power supply module
  AnS series power supply module A-20
  Q series power supply module A-20
  Redundant power supply module A-20
  Slim type power supply module A-20
Precautions
  Communication made by program 4-46
  Communication using auto refresh 4-20
  Design precautions A-2
  Disposal precautions. A-9
  Installation precautions A-4

Precautions for system configuration 2-49
Startup and maintenance precautions A-7
Transportation precautions App-1
Wiring precautions A-5
Process CPU A-19
Processing time 5-1
Program example
Continuous data transmission 8-31,8-37
Continuous data writing/reading using the user setting area 8-33,8-39
Sending bit and word data 8-30,8-36
PX Developer 2-46

[Q]

Q series A-19
Q series power supply module A-20
Q3□B A-19
Q3□RB A-19
Q3□SB A-19
Q5□B A-19
Q6□B A-19
Q6□RB A-19
QA1S6□B A-20
QA6ADP+A5□B/A6□B A-20
QA6□B A-20

[R]

Read instruction 4-39
Reducing processing time 5-10
Redundant system
Redundant base unit A-20
Redundant CPU A-19
Redundant extension base unit A-20
Redundant main base unit A-20
Redundant power supply module A-20
Refresh setting 4-11,6-8
Resetting the multiple CPU system 3-28,3-29
Restricted system area 4-3,4-7

[S]

S(P).CHGA 4-49
S(P).CHGT 4-49
S(P).CHGV 4-49
S(P).DDRD 4-51
S(P).DDWR 4-51
S(P).SFCS 4-49
S(P).SVST 4-49
S.GINT 4-53
Serial number 2-43
Slim type main base unit A-20
Slim type power supply module A-20
System configuration
Configurable device and available software . . 2-42
Configuration of peripheral devices 2-38
Precautions for system configuration 2-49
System recovery procedure 3-32

[U]

User setting area 4-3,4-7

[W]

Write instruction 4-39

WARRANTY

Please confirm the following product warranty details before using this product.

1. Gratis Warranty Term and Gratis Warranty Range

If any faults or defects (hereinafter "Failure") found to be the responsibility of Mitsubishi occurs during use of the product within the gratis warranty term, the product shall be repaired at no cost via the sales representative or Mitsubishi Service Company.
However, if repairs are required onsite at domestic or overseas location, expenses to send an engineer will be solely at the customer's discretion. Mitsubishi shall not be held responsible for any re-commissioning, maintenance, or testing on-site that involves replacement of the failed module.

[Gratis Warranty Term]

The gratis warranty term of the product shall be for one year after the date of purchase or delivery to a designated place.
Note that after manufacture and shipment from Mitsubishi, the maximum distribution period shall be six (6) months, and the longest gratis warranty term after manufacturing shall be eighteen (18) months. The gratis warranty term of repair parts shall not exceed the gratis warranty term before repairs.

[Gratis Warranty Range]

(1) The range shall be limited to normal use within the usage state, usage methods and usage environment, etc., which follow the conditions and precautions, etc., given in the instruction manual, user's manual and caution labels on the product.
(2) Even within the gratis warranty term, repairs shall be charged for in the following cases.
1. Failure occurring from inappropriate storage or handling, carelessness or negligence by the user. Failure caused by the user's hardware or software design.
2. Failure caused by unapproved modifications, etc., to the product by the user.
3. When the Mitsubishi product is assembled into a user's device, Failure that could have been avoided if functions or structures, judged as necessary in the legal safety measures the user's device is subject to or as necessary by industry standards, had been provided.
4. Failure that could have been avoided if consumable parts (battery, backlight, fuse, etc.) designated in the instruction manual had been correctly serviced or replaced.
5. Failure caused by external irresistible forces such as fires or abnormal voltages, and Failure caused by force majeure such as earthquakes, lightning, wind and water damage.
6. Failure caused by reasons unpredictable by scientific technology standards at time of shipment from Mitsubishi.
7. Any other failure found not to be the responsibility of Mitsubishi or that admitted not to be so by the user.

2. Onerous repair term after discontinuation of production

(1) Mitsubishi shall accept onerous product repairs for seven (7) years after production of the product is discontinued.
Discontinuation of production shall be notified with Mitsubishi Technical Bulletins, etc.
(2) Product supply (including repair parts) is not available after production is discontinued.

3. Overseas service

Overseas, repairs shall be accepted by Mitsubishi's local overseas FA Center. Note that the repair conditions at each FA Center may differ.

4. Exclusion of loss in opportunity and secondary loss from warranty liability

Regardless of the gratis warranty term, Mitsubishi shall not be liable for compensation of damages caused by any cause found not to be the responsibility of Mitsubishi, loss in opportunity, lost profits incurred to the user by Failures of Mitsubishi products, special damages and secondary damages whether foreseeable or not , compensation for accidents, and compensation for damages to products other than Mitsubishi products, replacement by the user, maintenance of on-site equipment, start-up test run and other tasks.

5. Changes in product specifications

The specifications given in the catalogs, manuals or technical documents are subject to change without prior notice.

6. Product application

(1) In using the Mitsubishi MELSEC programmable logic controller, the usage conditions shall be that the application will not lead to a major accident even if any problem or fault should occur in the programmable logic controller device, and that backup and fail-safe functions are systematically provided outside of the device for any problem or fault.
(2) The Mitsubishi programmable logic controller has been designed and manufactured for applications in general industries, etc.
Thus, applications in which the public could be affected such as in nuclear power plants and other power plants operated by respective power companies, and applications in which a special quality assurance system is required, such as for Railway companies or Public service purposes shall be excluded from the programmable logic controller applications.
In addition, applications in which human life or property that could be greatly affected, such as in aircraft, medical applications, incineration and fuel devices, manned transportation, equipment for recreation and amusement, and safety devices, shall also be excluded from the programmable logic controller range of applications.
However, in certain cases, some applications may be possible, providing the user consults their local Mitsubishi representative outlining the special requirements of the project, and providing that all parties concerned agree to the special circumstances, solely at the users discretion.

QCPU

User's Manual (Multiple CPU System)

MODEL	QCPU-U-MA-E
MODEL CODE	13JR75
SH(NA)-080485ENG-E(0708)MEE	

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