

Instruction Execution Times

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Introduction

This appendix contains several tables that provide the instruction execution times for the DL330, DL330P, and DL340 CPUs. One thing you will notice is that many of the execution times depend on the type of data being used with the instruction. For example, some of the instructions have different execution times if you use a regular data register instead of a constant.

You'll also notice that some of the data instructions (such as DSTR) require differing amounts of execution time depending on the type of data. There are generally three options.

- Data Registers
- I/O Data Registers
- Constants

The following paragraphs may help you understand the differences between the register types.

Data Registers

Some data registers are primarily used to hold variable data and are considered true data registers. For example, the registers that store the timer or counter current values, or just regular variable data would be considered as a data register. Don't think that you cannot load a bit pattern into these types of registers, you can. It's just that their primary use is as a data register. The following locations are considered as data registers.

| Type of Data | DL330 | DL330P | DL340 |
|--------------------------------|-------------|-------------|----------------------------|
| Timer / Counter Current Values | R600 – R677 | R600 – R677 | R600 – R677 |
| User Data Words | R400 – R563 | R400 – R563 | R400 – R563 R700 – R767 |

I/O Data Registers

You may recall that the I/O points are automatically mapped into data register locations. The following locations that contain this data are considered I/O registers and will take longer to execute with most instructions.

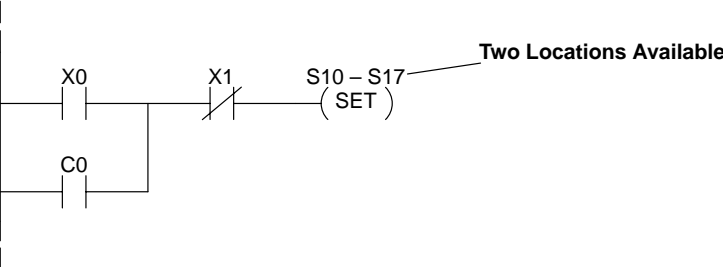
| Type of Data | DL330 | DL330P | DL340 |
|--------------|------------------------------|-----------------------------|-----------------------------|
| I/O Points | R000 – R016* R070 – R 076 | R000 – R016* R070 – R076 | R000 – R017* R070 – R076 |

NOTE: 160 – 167 can be used as I/O in a DL330 or DL330P CPU under certain conditions. 160 – 177 can be used as I/O in a DL340 CPU under certain conditions. You should consult Chapter 4 to determine which configurations allow the use of these points.

These points are normally used as control relays. You cannot use them as both control relays and as I/O points. Also, if you use these points as I/O, you cannot access these I/O points as a Data Register reference.

How to Read the Tables

Some of the instructions can have more than one parameter so the table shows execution times that depend on the amount and type of parameters. For example, the when you use the SET instruction to set a range of stages in a DL330P CPU, the execution time depends on how many stages are being set by the instruction.



| Instruction | Stage Instruction | | Stage Instruction not activated by a Jump instruction (ex. power flow) |
|-------------|---------------------------------------|--------------------|--|
| SET SG | $26.3 + 13.1\mu\text{s} \times (n-1)$ | 18.8 μs | Does not apply |
| RST SG | $26.3 + 13.1\mu\text{s} \times (n-1)$ | 18.8 μs | Does not apply |

Execution depends on numbers of locations and types of data used

DL330 Instruction Execution Times

Basic Input Instructions

| Instruction | Execute | Disabled by MCR |
|-------------------------------|--------------|-----------------|
| STR | 6.6 μ s | N/A |
| STR NOT | 9.1 μ s | N/A |
| AND | 5.3 μ s | N/A |
| AND NOT | 8.4 μ s | N/A |
| OR | 6.6 μ s | N/A |
| OR NOT | 9.1 μ s | N/A |
| STR T/C | 10.3 μ s | N/A |
| STR NOT T/C | 12.8 μ s | N/A |
| AND T/C | 5.3 μ s | N/A |
| AND NOT T/C | 8.4 μ s | N/A |
| OR T/C | 6.6 μ s | N/A |
| OR NOT T/C | 9.1 μ s | N/A |
| STR (Comparative Contact) | 50.9 μ s | N/A |
| STR NOT (Comparative Contact) | 61.5 μ s | N/A |
| AND (Comparative Contact) | 59.1 μ s | 6.2 μ s |
| AND NOT (Comparative Contact) | 60.3 μ s | 6.2 μ s |
| OR (Comparative Contact) | 60.3 μ s | 6.2 μ s |
| OR NOT (Comparative Contact) | 62.5 μ s | 6.2 μ s |
| AND STR | 3.8 μ s | N/A |
| OR STR | 3.8 μ s | N/A |
| MCR | 5.0 μ s | N/A |
| MCS | 3.0 μ s | N/A |

Output Type Instructions

| Instruction | Execute | Not Executed |
|-------------|--------------|--------------|
| OUT | 7.5 μ s | 7.5 μ s |
| SET OUT | 10.0 μ s | 10.0 μ s |
| SET | 17.5 μ s | 17.5 μ s |
| RST | 9.3 μ s | 9.3 μ s |
| SET OUT RST | 19.3 μ s | 19.3 μ s |

**Timer, Counters,
and Shift Registers**

| Instruction | Execute w/ Constant | Execute w/ Data Register | Execute w/ I/O Register | Not Executed |
|-------------|--|-----------------------------|----------------------------|-----------------|
| TMR | 90.9 μ s | 458.8 μ s | 700.0 μ s | 27.1 μ s |
| CNT | 92.9 μ s | 465.6 μ s | 706.8 μ s | 27.1 μ s |
| SR | 64.1 μ s+16.6 μ s times (# of shifts) | | | 53.1 μ s |

Data Operations

| Instruction | | Execute w/ Data Register | Execute w/ I/O Register | Execute w/ Constant | Not Executed |
|-------------|-----|---|----------------------------|------------------------|-----------------|
| DSTR | F50 | 80.7 μ s | 321.9 μ s | 14.3 μ s | 6.3 μ s |
| DSTR1 | F51 | 63.8 μ s | 140.9 μ s | N/A | 6.3 μ s |
| DSTR2 | F52 | 95.0 μ s | 172.2 μ s | N/A | 6.3 μ s |
| DSTR3 | F53 | 96.6 μ s | 173.8 μ s | N/A | 6.3 μ s |
| DSTR5 | F55 | N/A | 326.2 μ s | N/A | 6.3 μ s |
| DOUT | F60 | 52.6 μ s | 329.4 μ s | N/A | 6.3 μ s |
| DOUT1 | F61 | 39.1 μ s | 160.1 μ s | N/A | 6.3 μ s |
| DOUT2 | F62 | 39.8 μ s | 116.0 μ s | N/A | 6.3 μ s |
| DOUT3 | F63 | 55.0 μ s | 108.1 μ s | N/A | 6.3 μ s |
| DOUT5 | F65 | N/A | 358.3 μ s | N/A | 6.3 μ s |
| CMP<=> | F70 | 112.8 μ s | 354.0 μ s | 57.0 μ s | 6.3 μ s |
| ADD | F71 | 456.8 μ s | 698.0 μ s | 262.0 μ s | 6.3 μ s |
| SUB | F72 | 315.8 μ s | 557.0 μ s | 275.0 μ s | 6.3 μ s |
| MUL | F73 | 290–2664 μ s | 497–2851 μ s | 223–2576 μ s | 6.3 μ s |
| DIV | F74 | 742–2645 μ s | 1218–2851 μ s | 720–2557 μ s | 6.3 μ s |
| DAND | F75 | 103.7 μ s | 345.0 μ s | 55.6 μ s | 6.3 μ s |
| DOR | F76 | 103.7 μ s | 345.0 μ s | 55.6 μ s | 6.3 μ s |
| SHFR | F80 | 216 μ s+13.4 μ s times (# of shifts) | | | 6.3 μ s |
| SHFL | F81 | 220 μ s+13.4 μ s times (# of shifts) | | | 6.3 μ s |
| DECO | F82 | 56.3 μ s | N/A | N/A | 6.3 μ s |
| ENCO | F83 | 282.0 μ s | N/A | N/A | 6.3 μ s |
| INV | F84 | 30.0 μ s | N/A | N/A | 6.3 μ s |
| BIN | F85 | 412.2 μ s | N/A | N/A | 6.3 μ s |
| BCD | F86 | 746.0 μ s | N/A | N/A | 6.3 μ s |
| FAULT | F20 | 114.0 μ s | 355.3 μ s | 72.2 μ s | 6.3 μ s |

DL330P Instruction Execution Times

Basic Input Instructions

| Instruction | I/O, Control Relay | | Stage | | Timer / Counter | |
|-------------|--------------------|---------------|---------------|---------------|-----------------|--------------|
| | Executed | Not Executed | Executed | Not Executed | Executed | Not Executed |
| | * ** | * ** | * ** | * ** | * ** | * ** |
| STR | 28.4 / 31.4μs | 21.3 μs | 25.6 / 30.9μs | 22.2 μs | 121.3/117.8μs | 28.4 μs |
| STR NOT | 28.4 / 31.4μs | 21.3 μs | 25.6 / 30.9μs | 22.2 μs | 121.3/117.8μs | 28.4 μs |
| AND | 13.4 / 20.0μs | 13.4 / 20.0μs | 13.4 / 20.0μs | 13.4 / 20.0μs | 123.1/119.6μs | 20.3 μs |
| AND NOT | 18.1 / 21.6μs | 10.3 μs | 18.1 / 21.6μs | 10.3 μs | 123.1/119.6μs | 20.3 μs |
| OR | 21.8 / 25.3μs | 14.7 μs | 21.8 / 25.3μs | 14.7 μs | 123.1/119.6μs | 20.3 μs |
| OR NOT | 20.6 / 24.1μs | 14.7 μs | 20.6 / 24.1μs | 14.7 μs | 123.1/119.6μs | 20.3 μs |

* Execution time when data type is ON. For example, STR 000 takes 28.4 μs if point 000 is on.

** Execution time when data type is OFF. For example, STR 000 takes 31.4 μs if point 000 is off.

| Instruction | Executed | Not Executed |
|-------------|----------|--------------|
| AND STR | 25.9 μs | 22.8 μs |
| OR STR | 25.9 μs | 22.8 μs |

Output Type Instructions

| Instruction | Execute | Not Executed |
|-------------|---------|--------------|
| OUT | 20.6 μs | 20.6 μs |
| SET OUT | 24.3 μs | 16.6 μs |
| SET | 24.3 μs | 16.6 μs |
| RST | 24.3 μs | 16.6 μs |
| SET OUT RST | 33.8 μs | 29.4 μs |

Timer, Counters, and Shift Registers

| Instruction | Execute | Not Executed |
|-------------|-------------------------------|--------------|
| TMR | 92.8 μs | 50.9 μs |
| CNT | 97.5 μs | 46.3 μs |
| RST CNT | 25.9 μs | 16.6 μs |
| SR | 75.9 + 11.5μs x (# of shifts) | 41.9 μs |

Stage Instructions

| Instruction | Stage Instruction | | Stage Instruction not activated by a Jump instruction (ex. power flow) | |
|-------------|---------------------------------------|--------------|--|--------------|
| | Executed | Not Executed | Executed | Not Executed |
| ISG | 35.3 μ s | 20.0 μ s | 50.9 μ s | 30.6 μ s |
| SG | 35.3 μ s | 20.0 μ s | 50.9 μ s | 30.6 μ s |
| JMP | 28.4 μ s | 16.6 μ s | Does not apply | |
| NJMP | 40.3 μ s | 28.4 μ s | Does not apply | |
| SET SG | $26.3 + 13.1\mu\text{s} \times (n-1)$ | 18.8 μ s | Does not apply | |
| RST SG | $26.3 + 13.1\mu\text{s} \times (n-1)$ | 18.8 μ s | Does not apply | |

Data Operation Instructions

| Instruction | | Execute w/ Data Register | Execute w/ I/O Register | Execute w/ Constant | Not Executed |
|-------------|-----|---|----------------------------|------------------------|--------------|
| DSTR | F50 | 80.7 μ s | 321.9 μ s | 14.3 μ s | 6.3 μ s |
| DSTR1 | F51 | 63.8 μ s | 140.9 μ s | N/A | 6.3 μ s |
| DSTR2 | F52 | 95.0 μ s | 172.2 μ s | N/A | 6.3 μ s |
| DSTR3 | F53 | 96.6 μ s | 173.8 μ s | N/A | 6.3 μ s |
| DSTR5 | F55 | N/A | 326.2 μ s | N/A | 6.3 μ s |
| DOUT | F60 | 52.6 μ s | 329.4 μ s | N/A | 6.3 μ s |
| DOUT1 | F61 | 39.1 μ s | 160.1 μ s | N/A | 6.3 μ s |
| DOUT2 | F62 | 39.8 μ s | 116.0 μ s | N/A | 6.3 μ s |
| DOUT3 | F63 | 55.0 μ s | 108.1 μ s | N/A | 6.3 μ s |
| DOUT5 | F65 | N/A | 358.3 μ s | N/A | 6.3 μ s |
| CMP<=> | F70 | 112.8 μ s | 354.0 μ s | 57.0 μ s | 6.3 μ s |
| ADD | F71 | 456.8 μ s | 698.0 μ s | 262.0 μ s | 6.3 μ s |
| SUB | F72 | 315.8 μ s | 557.0 μ s | 275.0 μ s | 6.3 μ s |
| MUL | F73 | 290–2664 μ s | 497–2851 μ s | 223–2576 μ s | 6.3 μ s |
| DIV | F74 | 742–2645 μ s | 1218–2851 μ s | 720–2557 μ s | 6.3 μ s |
| DAND | F75 | 103.7 μ s | 345.0 μ s | 55.6 μ s | 6.3 μ s |
| DOR | F76 | 103.7 μ s | 345.0 μ s | 55.6 μ s | 6.3 μ s |
| SHFR | F80 | 216 μ s+13.4 μ s times (# of shifts) | | | 6.3 μ s |
| SHFL | F81 | 220 μ s+13.4 μ s times (# of shifts) | | | 6.3 μ s |
| DECO | F82 | 56.3 μ s | N/A | N/A | 6.3 μ s |
| ENCO | F83 | 282.0 μ s | N/A | N/A | 6.3 μ s |
| INV | F84 | 30.0 μ s | N/A | N/A | 6.3 μ s |
| BIN | F85 | 412.2 μ s | N/A | N/A | 6.3 μ s |
| BCD | F86 | 746.0 μ s | N/A | N/A | 6.3 μ s |
| FAULT | F20 | 114.0 μ s | 355.3 μ s | 72.2 μ s | 6.3 μ s |

DL340 Instruction Execution Times

Basic Input Instructions

| Instruction | Execute | Disabled by MCR |
|-------------|---------------|-----------------|
| STR | 0.875 μ s | N/A |
| STR NOT | 1.750 μ s | N/A |
| AND | 0.625 μ s | N/A |
| AND NOT | 1.5 μ s | N/A |
| OR | 1.125 μ s | N/A |
| OR NOT | 1.75 μ s | N/A |
| STR T/C | 0.875 μ s | N/A |
| STR NOT T/C | 1.75 μ s | N/A |
| AND T/C | 0.625 μ s | N/A |
| AND NOT T/C | 1.5 μ s | N/A |
| OR T/C | 1.125 μ s | N/A |
| OR NOT T/C | 1.75 μ s | N/A |
| AND STR | 0.75 μ s | N/A |
| OR STR | 0.75 μ s | N/A |
| MCR | 0.75 μ s | N/A |
| MCS | 1.125 μ s | N/A |

Comparative Contacts

| Instructions | Execute w/ Data Register | Execute w/ I/O Register | Execute w/ Constant | | Not Executed |
|--------------|-----------------------------|----------------------------|------------------------|--------------|--------------|
| | | | RAM | EE / UV | |
| STR | 56.8 μ s | 95.0 μ s | 15.6 μ s | 15.6 μ s | N/ A |
| STR NOT | 56.8 μ s | 96.5 μ s | 15.6 μ s | 15.6 μ s | N/A |
| AND | 56.8 μ s | 95.0 μ s | 15.0 μ s | 15.0 μ s | 1.4 μ s |
| AND NOT | 56.8 μ s | 96.5 μ s | 15.6 μ s | 15.6 μ s | 1.4 μ s |
| OR | 56.8 μ s | 94.0 μ s | 15.6 μ s | 15.6 μ s | 1.4 μ s |
| OR NOT | 56.8 μ s | 94.0 μ s | 16.2 μ s | 16.2 μ s | 1.4 μ s |

Output Type Instructions

| Instruction | Execute | Not Executed |
|-------------|---------------|---------------|
| OUT | 1.188 μ s | 1.188 μ s |
| SET OUT | 1.563 μ s | 1.563 μ s |
| SET | 1.625 μ s | 1.4 μ s |
| RST | 1.625 μ s | 1.4 μ s |
| SET OUT RST | 7.5 μ s | 7.125 μ s |

**Timer, Counters,
and Shift Registers**

| Instructions | Execute w/ Data Register | Execute w/ I/O Register | Execute w/ Constant | | Not Executed |
|--------------|---|----------------------------|------------------------|--------------|-----------------|
| | | | RAM | EE / UV | |
| TMR | 68.1 μ s | 113.8 μ s | 22.5 μ s | 22.5 μ s | 15.7 μ s |
| CNT | 67.3 μ s | 97.9 μ s | 22.5 μ s | 22.5 μ s | 25.6 μ s |
| SR | 21.8 μ s+3.8 μ s times (# of shifts) | | | | 8.3 μ s |

**Data Operation
Instructions**

| Instruction | | Execute w/ Data Register | Execute w/ I/O Register | Execute w/ Constant | Not Executed |
|-------------|-----|---|----------------------------|------------------------|-----------------|
| DSTR | F50 | 29.4 μ s | 60.6 μ s | 10.6 μ s | 1.4 μ s |
| DSTR1 | F51 | 24.3 μ s | 39.4 μ s | N/A | 1.4 μ s |
| DSTR2 | F52 | 25.0 μ s | 40.6 μ s | N/A | 1.4 μ s |
| DSTR3 | F53 | 96.6 μ s | 39.4 μ s | N/A | 1.4 μ s |
| DSTR5 | F55 | N/A | 76.8 μ s | N/A | 1.4 μ s |
| DOUT | F60 | 18.8 μ s | 53.8 μ s | N/A | 1.4 μ s |
| DOUT1 | F61 | 13.1 μ s | 33.1 μ s | N/A | 1.4 μ s |
| DOUT2 | F62 | 16.3 μ s | 23.1 μ s | N/A | 1.4 μ s |
| DOUT3 | F63 | 15.6 μ s | 23.1 μ s | N/A | 1.4 μ s |
| DOUT5 | F65 | N/A | 59.3 μ s | N/A | 1.4 μ s |
| CMP<=> | F70 | 30.0 μ s | 61.8 μ s | 15.6 μ s | 1.4 μ s |
| ADD | F71 | 77.5 μ s | 108.0 μ s | 63.0 μ s | 1.4 μ s |
| SUB | F72 | 70.6 μ s | 101.8 μ s | 57.0 μ s | 1.4 μ s |
| MUL | F73 | 71.8 – 540.0 μ s | 102.5 – 571.2 μ s | 58.7 – 526.8 μ s | 1.4 μ s |
| DIV | F74 | 73.7 – 568.1 μ s | 104.3 – 598.7 μ s | 58.7 – 553.1 μ s | 1.4 μ s |
| DAND | F75 | 29.3 μ s | 60.0 μ s | 15.6 μ s | 1.4 μ s |
| DOR | F76 | 31.2 μ s | 62.5 μ s | 15.6 μ s | 1.4 μ s |
| SHFR | F80 | 18.1 μ s+2.5 μ s times (# of shifts) | | | 1.4 μ s |
| SHFL | F81 | 18.1 μ s+2.5 μ s times (# of shifts) | | | 1.4 μ s |
| DECO | F82 | 15.6 μ s | N/A | N/A | 1.4 μ s |
| ENCO | F83 | 47.5 μ s | N/A | N/A | 1.4 μ s |
| INV | F84 | 6.8 μ s | N/A | N/A | 1.4 μ s |
| BIN | F85 | 48.1 μ s | N/A | N/A | 1.4 μ s |
| BCD | F86 | 88.7 – 326.0 μ s | N/A | N/A | 1.4 μ s |
| FAULT | F20 | 28.8 μ s | 60.1 μ s | 15.0 μ s | 1.4 μ s |