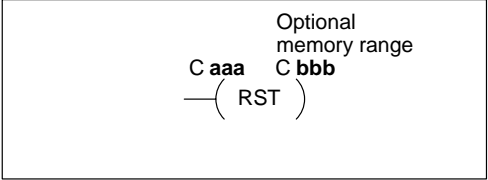


Reset Counter
(RST)
DL330P Only

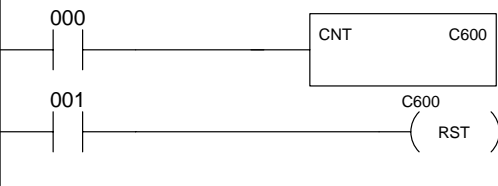
The Reset Counter instruction used in the DL330P CPU provides a reset for the counter instruction. One counter or a range of counters can be reset.



Operand Data Type	D3-330 Range		D3-340 Range		D3-330P Range	
	aaa	bbbb	aaa	bbbb	aaa	bbbb
Counters	—	—	—	—	600-677	600-677

In the following Reset Counter example when input contact 001 is on the Reset Counter instruction will reset counter 600.

DirectSOFT Display



Handheld Programmer Keystrokes

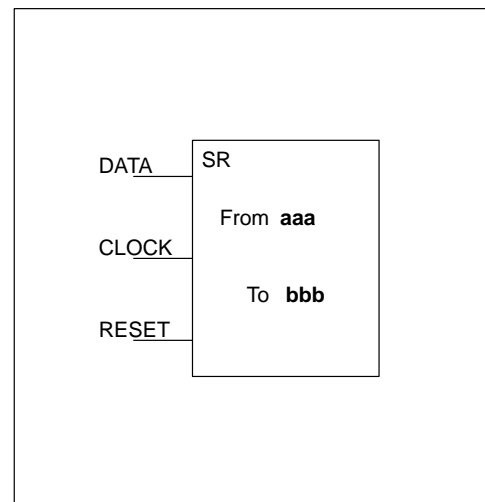
STR	SHF	0	ENT			
CNT	SHF	6	0	0	ENT	
STR	SHF	1	ENT			
RST	CNT	SHF	6	0	0	ENT

Shift Register (SR) DL330P Only

The Shift Register instruction shifts data through a predefined number of control relays. There are 77 control relays which can be used for internal control relays or shift register bits. There is no limit to the number of shift registers which can be used in a program, however the total number of bits used cannot exceed 77.

The Shift Register has three input contacts.

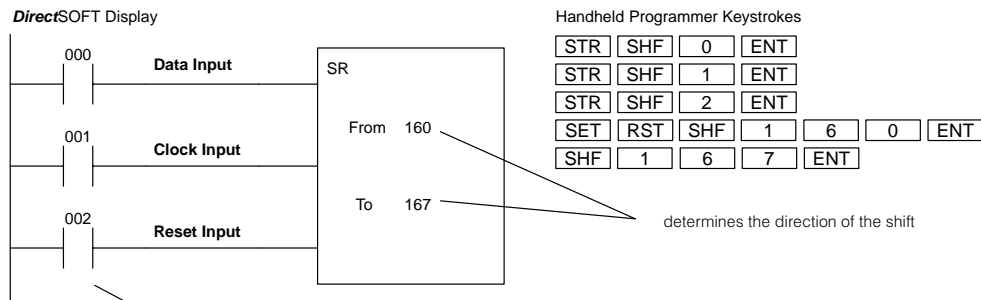
- Data — determines the value (1 or 0) that will enter the register
- Clock — shifts the bits one position on each low to high transition
- Reset — resets the Shift Register to all zeros.



With each off to on transition of the clock input, the bits which make up the shift register block are shifted by one bit position and the status of the data input is placed into the starting bit position of the shift register. The direction of the shift depends on the entry in the From and To fields. From 160 to 167 would define a shift right block of eight bits to be shifted from bit left to right. From 167 to 160 would define a shift left block of eight bits, but would shift from right to left. The maximum size of the shift register block is limited to 77 bits. There is no minimum block size.

Operand Data Type	D3-330 Range		D3-340 Range		D3-330P Range	
	aaa	bbbb	aaa	bbbb	aaa	bbbb
Shift Register Bits	—	—	—	—	160-174 200-277	160-174 200-277

In the following example, when the clock input transitions from low to high the value in the Data input is placed in the first bit position of the shift register and the successive successive bits are shifted to the right. When the Reset input transitions from low to high the entire shift register is set to zeros.



Inputs on Successive Scans

Shift Register Bits

Data	Clock	Reset		160	167
1	1	0	—	1	
0	1	0	—	0	
0	1	0	—		0
1	1	0	—	1	0
0	1	0	—	0	1
0	0	1	—		