C

Instruction Execution Times

In This Appendix. . . .

Introduction

This appendix contains several tables that provide the instruction execution times for the DL430, DL440, and DL450 CPUs. Many execution times depend on the type of data used with the instruction. Registers are classified into the following types:

- Data (word) Registers
- Bit Registers

V-Memory Data Registers

Some V-memory locations are considered data registers, such as timer or counter current values. Standard User V-memory is classified as a V-memory data register. Note that can load a bit pattern into these types of registers, even though their primary use is for data registers. The following locations are data registers:

Data Registers	DL430	DL440	DL450
Timer Current Values	V00000 – V 00177	V00000 – V00377	V00000 – V00377
Counter Current Values	V01000 – V01177	V01000 – V01177	V01000 – V01377
User Data Words	V1400 – V7377	V1400 – V7377 V10000 – V17777	V1400 – V7377 V10000 – V37777

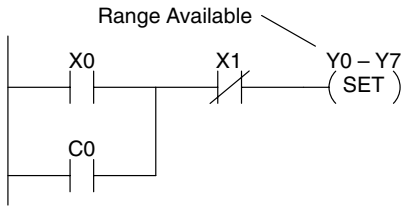
V-Memory Bit Registers

You may recall some of the discrete points such as X, Y, C, etc. are automatically mapped into V memory. The following bit registers contain this data:

Bit Registers	DL430	DL440	DL450
Input Points (X)	V40400 – V 40423	V40400 – V 40423	V40400 – V 40477
Output Points (Y)	V40500 – V40523	V40500 – V40523	V40500 – V40577
Control Relays (C)	V40600 – V40635	V40600 – V40677	V40600 – V40777
Timer Status Bits	V41100 – V41107	V41100 – V41117	V41100 – V41117
Counter Status Bits	V41140 – V41147	V41140 – V41147	V41140 – V41157
Stages	V41000 – V41027	V41000 – V41077	V41000 – V41077
Remote I/O, (Global GX) (Global GY)	V40000 – V40037	V40000 – V40077	V40000 – V40177 V40200 – V40377

How to Read the Tables

Some instructions can have more than one parameter. For example, the SET instruction shown in the ladder program to the right can set a single point or a range of points.



In these cases, execution times depend on the amount and type of parameters. The execution time tables list execution times for various situations, as shown below:

SET	1st #:	X, Y, C, S, GX, GY	20.8 µs
	2nd #:	X, Y, C, S, GX, GY (N pt)	13.0µs+7.8µsxN
RST	1st #:	X, Y, C, S, GX, GY	19.5 µs
	2nd #:	X, Y, C, S, GX, GY (N pt)	11.7µs+7.8µsxN

Execution depends on numbers of locations and types of data used

NOTE: The GY data type listed for some instructions throughout this appendices is valid only for the DL450 CPU, which uses both GX and GY data types for Remote I/O points. The DL430 and DL440 CPUs use the GX data type for any Remote I/O points.

Boolean Instructions

Boolean Instructions		DL430		DL440		DL450	
Instruction	Legal Data Types	Execute	Not Exe.	Execute	Not Exe.	Execute	Not Exe.
STR	X, Y, C, T, CT	4.7 µs	4.7 µs	0.33 µs	0.33 µs	0.96 µs	0.96 µs
	S, SP, GX, GY	4.7 µs	4.7 µs	8.0 µs	8.0 µs	1.0 µs	1.0 µs
STRN	X, Y, C, T, CT	5.7 µs	5.7 µs	0.33 µs	0.33 µs	1.0 µs	1.0 µs
	S, SP, GX, GY	5.7 µs	5.7 µs	8.0 µs	8.0 µs	1.0 µs	1.0 µs
STRB	V:Register (Bit)	—	—	—	—	5.0 µs	??? µs
	P:Indirect (Bit)	—	—	—	—	15.3 µs	??? µs
STRNB	V:Register (Bit)	—	—	—	—	4.9 µs	??? µs
	P:Indirect (Bit)	—	—	—	—	15.1 µs	??? µs
OR	X, Y, C, T, CT	3.1 µs	3.1 µs	0.33 µs	0.33 µs	0.9 µs	0.9 µs
	S, SP, GX, GY	3.1 µs	3.1 µs	4.24 µs	4.24 µs	0.9 µs	0.9 µs
ORN	X, Y, C, CT	4.1 µs	4.1 µs	0.33 µs	0.33 µs	0.96 µs	0.96 µs
	S, SP, GX, GY	4.1 µs	4.1 µs	4.67 µs	4.67 µs	0.96 µs	0.96 µs
ORB	V:Register (Bit)	—	—	—	—	4.7 µs	??? µs
	P:Indirect (Bit)	—	—	—	—	15.0 µs	??? µs
ORNB	V:Register (Bit)	—	—	—	—	4.6 µs	??? µs
	P:Indirect (Bit)	—	—	—	—	14.8 µs	??? µs
AND	X, Y, C, T, CT	2.4 µs	2.4 µs	0.33 µs	0.33 µs	0.8 µs	0.8 µs
	S, SP, GX, GY	2.4 µs	2.4 µs	2.72 µs	2.72 µs	0.8 µs	0.8 µs
ANDN	X, Y, C, T, CT	3.4 µs	3.4 µs	0.33 µs	0.33 µs	0.9 µs	0.9 µs
	S, SP, GX, GY	3.4 µs	3.4 µs	3.14 µs	3.14 µs	0.9 µs	0.9 µs
ANDB	V:Register (Bit)	—	—	—	—	4.6 µs	??? µs
	P:Indirect (Bit)	—	—	—	—	14.8 µs	??? µs
ANDNB	V:Register (Bit)	—	—	—	—	4.4 µs	??? µs
	P:Indirect (Bit)	—	—	—	—	14.7 µs	??? µs
ANDSTR	None	1.8 µs	1.8 µs	0.33 µs	0.33 µs	0.5 µs	0.5 µs
ORSTR	None	1.8 µs	1.8 µs	0.33 µs	0.33 µs	0.5 µs	0.5 µs
OUT	X, Y, C	6.7 µs	6.7 µs	0.33 µs	0.33 µs	2.9 µs	2.9 µs
	GX, GY	6.7 µs	6.7 µs	2.06 µs	2.06 µs	2.9 µs	2.9 µs
OUTB	V:Register (Bit)	—	—	—	—	5.6 µs	??? µs
	P:Indirect (Bit)	—	—	—	—	16.4 µs	??? µs
OROUT	X, Y, C, GX, GY	8.3 µs	8.3 µs	6.1 µs	6.1 µs	3.4 µs	3.4 µs
NOT	None	—	—	3.2 µs	—	**???** µs	—

Boolean Instructions		DL430		DL440		DL450	
Instruction	**Legal Data Types**	**Execute**	**Not Exe.**	**Execute**	**Not Exe.**	**Execute**	**Not Exe.**
PD	X, Y, C	15.1 µs	15.1 µs	8.5 µs	8.5 µs	10.0 µs	10.0 µs
STRPD	X, Y, C, T, CT, S, SP, GX, GY	—	—	—	—	3.7 µs	3.7 µs
STRND	X, Y, C, T, CT, S, SP, GX, GY	—	—	—	—	2.8 µs	2.8 µs
ANDPD	X, Y, C, T, CT, S, SP, GX, GY	—	—	—	—	3.6 µs	3.6 µs
ANDND	X, Y, C, T, CT, S, SP, GX, GY	—	—	—	—	2.7 µs	2.7 µs
ORPD	X, Y, C, T, CT, S, SP, GX, GY	—	—	—	—	3.6 µs	3.6 µs
ORND	X, Y, C, T, CT, S, SP, GX, GY	—	—	—	—	2.7 µs	2.7 µs
SET	1st #: X, Y, C	20.8 µs	5.2 µs	0.33 µs	0.33 µs	5.6 µs	1.0 µs
	S, GX, GY	20.8 µs	5.2 µs	14.6 µs	5.4 µs	5.6 µs	1.0 µs
	2nd #: X, Y, C, S, GX (N pt)	13.0 µs+ 7.8µsxN	5.2 µs	8.9 µs+ 5.7µsxN	5.4 µs	7.6 µs+ 0.6µsxN	1.2 µs
SETB	V:Register (Bit)	—	—	—	—	10.5 µs	2.3 µs
	P:Indirect (Bit)	—	—	—	—	22.2 µs	13.8 µs
RST	1st #: X, Y, C	19.5 µs	5.2 µs	0.33 µs	0.33 µs	5.6 µs	1.0 µs
	S, GX, GY	19.5 µs	5.2 µs	13.7 µs	4.5 µs	5.6 µs	5.6 µs
	2nd #: X, Y, C, S, GX, GY (N pt)	11.7 µs+ 7.8µsxN	5.2 µs	8.0 µs+ 5.7µsxN	4.5 µs	7.6 µs+ 0.6µsxN	1.2 µs
	1st #: T, CT	28.2 µs	5.2 µs	15.2 µs	3.8 µs	10.2 µs	0.9 µs
	2nd #: T, CT (N pt)	23.3 µs+ 5.8µsxN	5.2 µs	10.7 µs+ 4.6µsxN	3.8 µs	6.1 µs+ 1.9µsxN	1.2 µs
RSTB	V:Register (Bit)	—	—	—	—	10.5 µs	2.3 µs
	P:Indirect (Bit)	—	—	—	—	22.2 µs	13.8 µs
PAUSE	1wd: Y	24.0 µs	24.0 µs	14.7 µs	14.7 µs	7.4 µs	7.5 µs
	2wd: Y (N points)	18 µs+ 6µs x N	18µs+ 6µs x N	11µs+ 4µs x N	11µs+ 4µs x N	14.6µs+ 0.32µs xN	14.6µs+ 0.3µs x N

Comparative Boolean Instructions

Comparative Boolean (cont.)			DL430		DL440		DL450	
Instruction	**Legal Data Types**		**Execute**	**Not Execute**	**Execute**	**Not Execute**	**Execute**	**Not Execute**
STRE	1st	2nd						
	V: Data Reg.	V:Data Reg.	61 µs	13.5 µs	56 µs	12.2 µs	4.9 µs	4.9
		V:Bit Reg.	182 µs	13.5 µs	130 µs	12.2 µs	4.9 µs	4.9
		K:Constant	75 µs	13.5 µs	69 µs	12.2 µs	3.5 µs	3.5
		P:Indir. (Data)	—	—	178 µs	12.2 µs	9.9 µs	9.9
		P:Indir. (Bit)	—	—	270 µs	12.2 µs	9.9 µs	9.9
	V: Bit Reg.	V:Data Reg.	182 µs	13.5 µs	130 µs	12.2 µs	4.9 µs	4.9
		V:Bit Reg.	300 µs	13.5 µs	206 µs	12.2 µs	4.9 µs	4.9
		K:Constant	193 µs	13.5 µs	206 µs	12.2 µs	3.5 µs	3.5
		P:Indir. (Data)	—	—	252 µs	12.2 µs	9.9 µs	9.9
		P:Indir. (Bit)	—	—	347 µs	12.2 µs	9.9 µs	9.9
	P:Indir. (Data)	V:Data Reg.	—	—	174 µs	12.2 µs	3.4 µs	9.9
		V:Bit Reg.	—	—	248 µs	12.2 µs	3.4 µs	9.9
		K:Constant	—	—	182 µs	12.2 µs	8.3 µs	8.3
		P:Indir. (Data)	—	—	296 µs	12.2 µs	14.3 µs	14.3
		P:Indir. (Bit)	—	—	387 µs	12.2 µs	14.3 µs	14.3
	P:Indir. (Bit)	V:Data Reg.	—	—	265 µs	12.2 µs	3.4 µs	9.9
		V:Bit Reg.	—	—	341 µs	12.2 µs	3.4 µs	9.9
		K:Constant	—	—	276 µs	12.2 µs	8.3 µs	8.3
		P:Indir. (Data)	—	—	387 µs	12.2 µs	14.3 µs	14.3
		P:Indir. (Bit)	—	—	480 µs	12.2 µs	14.3 µs	14.3
STRNE	1st	2nd						
	V: Data Reg.	V:Data Reg.	63 µs	13.5 µs	56 µs	12.2 µs	4.9 µs	4.9
		V:Bit Reg.	180 µs	13.5 µs	130 µs	12.2 µs	4.9 µs	4.9
		K:Constant	77 µs	13.5 µs	69 µs	12.2 µs	3.5 µs	3.5
		P:Indir. (Data)	—	—	178 µs	12.2 µs	9.9 µs	9.9
		P:Indir. (Bit)	—	—	270 µs	12.2 µs	9.9 µs	9.9
	V: Bit Reg.	V:Data Reg.	180 µs	13.5 µs	130 µs	12.2 µs	4.9 µs	4.9
		V:Bit Reg.	298 µs	13.5 µs	206 µs	12.2 µs	4.9 µs	4.9
		K:Constant	195 µs	13.5 µs	206 µs	12.2 µs	3.5 µs	3.5
		P:Indir. (Data)	—	—	252 µs	12.2 µs	9.9 µs	9.9
		P:Indir. (Bit)	—	—	347 µs	12.2 µs	9.9 µs	9.9
	P:Indir. (Data)	V:Data Reg.	—	—	174 µs	12.2 µs	3.4 µs	9.9
		V:Bit Reg.	—	—	248 µs	12.2 µs	3.4 µs	9.9
		K:Constant	—	—	182 µs	12.2 µs	8.3 µs	8.3
		P:Indir. (Data)	—	—	296 µs	12.2 µs	14.3 µs	14.3
		P:Indir. (Bit)	—	—	387 µs	12.2 µs	14.3 µs	14.3
	P:Indir. (Bit)	V:Data Reg.	—	—	265 µs	12.2 µs	3.4 µs	9.9
		V:Bit Reg.	—	—	341 µs	12.2 µs	3.4 µs	9.9
		K:Constant	—	—	276 µs	12.2 µs	8.3 µs	8.3
		P:Indir. (Data)	—	—	387 µs	12.2 µs	14.3 µs	14.3
		P:Indir. (Bit)	—	—	480 µs	12.2 µs	14.3 µs	14.3

Comparative Boolean (cont.)			DL430		DL440		DL450	
Instruction	**Legal Data Types**		**Execute**	**Not Execute**	**Execute**	**Not Execute**	**Execute**	**Not Execute**
ORE	1st	2nd						
	V: Data Reg.	V:Data Reg.	62 µs	11.0 µs	48 µs	10.8 µs	4.9 µs	4.9 µs
		V:Bit Reg.	180 µs	11.0 µs	122 µs	10.8 µs	4.9 µs	4.9 µs
		K:Constant	73 µs	11.0 µs	55 µs	10.8 µs	3.5 µs	3.5 µs
		P:Indir. (Data)	—	—	170 µs	10.8 µs	9.9 µs	9.9 µs
		P:Indir. (Bit)	—	—	262 µs	10.8 µs	9.9 µs	9.9 µs
	V: Bit Reg.	V:Data Reg.	180 µs	11.0 µs	122 µs	10.8 µs	4.9 µs	4.9 µs
		V:Bit Reg.	297 µs	11.0 µs	198 µs	10.8 µs	4.9 µs	4.9 µs
		K:Constant	191 µs	11.0 µs	131 µs	10.8 µs	3.5 µs	3.5 µs
		P:Indir. (Data)	—	—	244 µs	10.8 µs	9.9 µs	9.9 µs
		P:Indir. (Bit)	—	—	340 µs	10.8 µs	9.9 µs	9.9 µs
	P:Indir. (Data)	V:Data Reg.	—	—	166 µs	10.8 µs	9.9 µs	9.9 µs
		V:Bit Reg.	—	—	240 µs	10.8 µs	9.9 µs	9.9 µs
		K:Constant	—	—	175 µs	10.8 µs	8.3 µs	8.3 µs
		P:Indir. (Data)	—	—	288 µs	10.8 µs	14.3 µs	14.3 µs
		P:Indir. (Bit)	—	—	379 µs	10.8 µs	14.3 µs	14.3 µs
	P:Indir. (Bit)	V:Data Reg.	—	—	257 µs	10.8 µs	9.9 µs	9.9 µs
		V:Bit Reg.	—	—	333 µs	10.8 µs	9.9 µs	9.9 µs
		K:Constant	—	—	268 µs	10.8 µs	8.3 µs	8.3 µs
		P:Indir. (Data)	—	—	380 µs	10.8 µs	14.3 µs	14.3 µs
		P:Indir. (Bit)	—	—	473 µs	10.8 µs	14.3 µs	14.3 µs
ORNE	1st	2nd						
	V: Data Reg.	V:Data Reg.	62 µs	11.0 µs	48 µs	10.8 µs	4.9 µs	4.9 µs
		V:Bit Reg.	178 µs	11.0 µs	122 µs	10.8 µs	4.9 µs	4.9 µs
		K:Constant	75 µs	11.0 µs	55 µs	10.8 µs	3.5 µs	3.5 µs
		P:Indir. (Data)	—	—	170 µs	10.8 µs	9.9 µs	9.9 µs
		P:Indir. (Bit)	—	—	262 µs	10.8 µs	9.9 µs	9.9 µs
	V: Bit Reg.	V:Data Reg.	178 µs	11.0 µs	122 µs	10.8 µs	4.9 µs	4.9 µs
		V:Bit Reg.	296 µs	11.0 µs	198 µs	10.8 µs	4.9 µs	4.9 µs
		K:Constant	192 µs	11.0 µs	131 µs	10.8 µs	3.5 µs	3.5 µs
		P:Indir. (Data)	—	—	244 µs	10.8 µs	9.9 µs	9.9 µs
		P:Indir. (Bit)	—	—	340 µs	10.8 µs	9.9 µs	9.9 µs
	P:Indir. (Data)	V:Data Reg.	—	—	166 µs	10.8 µs	9.9 µs	9.9 µs
		V:Bit Reg.	—	—	240 µs	10.8 µs	9.9 µs	9.9 µs
		K:Constant	—	—	175 µs	10.8 µs	8.3 µs	8.3 µs
		P:Indir. (Data)	—	—	288 µs	10.8 µs	14.3 µs	14.3 µs
		P:Indir. (Bit)	—	—	379 µs	10.8 µs	14.3 µs	14.3 µs
	P:Indir. (Bit)	V:Data Reg.	—	—	257 µs	10.8 µs	9.9 µs	9.9 µs
		V:Bit Reg.	—	—	333 µs	10.8 µs	9.9 µs	9.9 µs
		K:Constant	—	—	268 µs	10.8 µs	8.3 µs	8.3 µs
		P:Indir. (Data)	—	—	380 µs	10.8 µs	14.3 µs	14.3 µs
		P:Indir. (Bit)	—	—	473 µs	10.8 µs	14.3 µs	14.3 µs

Comparative Boolean (cont.)			DL430		DL440		DL450	
Instruction	**Legal Data Types**		**Execute**	**Not Execute**	**Execute**	**Not Execute**	**Execute**	**Not Execute**
ANDE	1st	2nd						
	V: Data Reg.	V:Data Reg.	60 µs	11.0 µs	48 µs	10.8 µs	4.9 µs	4.9 µs
		V:Bit Reg.	178 µs	11.0 µs	122 µs	10.8 µs	4.9 µs	4.9 µs
		K:Constant	74 µs	11.0 µs	55 µs	10.8 µs	3.5 µs	3.5 µs
		P:Indir. (Data)	—	—	170 µs	10.8 µs	9.9 µs	9.9 µs
		P:Indir. (Bit)	—	—	262 µs	10.8 µs	9.9 µs	9.9 µs
	V: Bit Reg.	V:Data Reg.	178 µs	11.0 µs	122 µs	10.8 µs	4.9 µs	4.9 µs
		V:Bit Reg.	296 µs	11.0 µs	198 µs	10.8 µs	4.9 µs	4.9 µs
		K:Constant	192 µs	11.0 µs	131 µs	10.8 µs	3.5 µs	3.5 µs
		P:Indir. (Data)	—	—	244 µs	10.8 µs	9.9 µs	9.9 µs
		P:Indir. (Bit)	—	—	340 µs	10.8 µs	9.9 µs	9.9 µs
	P:Indir. (Data)	V:Data Reg.	—	—	166 µs	10.8 µs	9.9 µs	9.9 µs
		V:Bit Reg.	—	—	240 µs	10.8 µs	9.9 µs	9.9 µs
		K:Constant	—	—	175 µs	10.8 µs	8.3 µs	8.3 µs
		P:Indir. (Data)	—	—	288 µs	10.8 µs	14.3 µs	14.3 µs
		P:Indir. (Bit)	—	—	379 µs	10.8 µs	14.3 µs	14.3 µs
	P:Indir. (Bit)	V:Data Reg.	—	—	257 µs	10.8 µs	9.9 µs	9.9 µs
		V:Bit Reg.	—	—	333 µs	10.8 µs	9.9 µs	9.9 µs
		K:Constant	—	—	268 µs	10.8 µs	8.3 µs	8.3 µs
		P:Indir. (Data)	—	—	380 µs	10.8 µs	14.3 µs	14.3 µs
		P:Indir. (Bit)	—	—	473 µs	10.8 µs	14.3 µs	14.3 µs
ANDNE	1st	2nd						
	V: Data Reg.	V:Data Reg.	62 µs	11.0 µs	48 µs	10.8 µs	4.9 µs	4.9 µs
		V:Bit Reg.	179 µs	11.0 µs	122 µs	10.8 µs	4.9 µs	4.9 µs
		K:Constant	73 µs	11.0 µs	55 µs	10.8 µs	3.5 µs	3.5 µs
		P:Indir. (Data)	—	—	170 µs	10.8 µs	9.9 µs	9.9 µs
		P:Indir. (Bit)	—	—	262 µs	10.8 µs	9.9 µs	9.9 µs
	V: Bit Reg.	V:Data Reg.	179 µs	11.0 µs	122 µs	10.8 µs	4.9 µs	4.9 µs
		V:Bit Reg.	297 µs	11.0 µs	198 µs	10.8 µs	4.9 µs	4.9 µs
		K:Constant	191 µs	11.0 µs	131 µs	10.8 µs	3.5 µs	3.5 µs
		P:Indir. (Data)	—	—	244 µs	10.8 µs	9.9 µs	9.9 µs
		P:Indir. (Bit)	—	—	340 µs	10.8 µs	9.9 µs	9.9 µs
	P:Indir. (Data)	V:Data Reg.	—	—	166 µs	10.8 µs	9.9 µs	9.9 µs
		V:Bit Reg.	—	—	240 µs	10.8 µs	9.9 µs	9.9 µs
		K:Constant	—	—	175 µs	10.8 µs	8.3 µs	8.3 µs
		P:Indir. (Data)	—	—	288 µs	10.8 µs	14.3 µs	14.3 µs
		P:Indir. (Bit)	—	—	379 µs	10.8 µs	14.3 µs	14.3 µs
	P:Indir. (Bit)	V:Data Reg.	—	—	257 µs	10.8 µs	9.9 µs	9.9 µs
		V:Bit Reg.	—	—	333 µs	10.8 µs	9.9 µs	9.9 µs
		K:Constant	—	—	268 µs	10.8 µs	8.3 µs	8.3 µs
		P:Indir. (Data)	—	—	380 µs	10.8 µs	14.3 µs	14.3 µs
		P:Indir. (Bit)	—	—	473 µs	10.8 µs	14.3 µs	14.3 µs

Comparative Boolean (cont.)			DL430		DL440		DL450	
Instruction	**Legal Data Types**		**Execute**	**Not Exe.**	**Execute**	**Not Exe.**	**Execute**	**Not Exe.**
STR	1st	2nd						
	T, CT	V:Data Reg.	65 µs	13.5 µs	56 µs	12.2 µs	4.8 µs	4.8 µs
		V:Bit Reg.	182 µs	13.5 µs	130 µs	12.2 µs	4.8 µs	4.8 µs
		K:Constant	75 µs	13.5 µs	63 µs	12.2 µs	3.4 µs	3.4 µs
		P:Indir. (Data)	—	—	178 µs	12.2 µs	9.9 µs	9.9 µs
		P:Indir. (Bit)	—	—	270 µs	12.2 µs	9.9 µs	9.9 µs
	1st	2nd						
	V: Data Reg.	V:Data Reg.	66 µs	13.5 µs	56 µs	12.2 µs	4.8 µs	4.8 µs
		V:Bit Reg.	184 µs	13.5 µs	130 µs	12.2 µs	4.8 µs	4.8 µs
		K:Constant	79 µs	13.5 µs	63 µs	12.2 µs	3.4 µs	3.4 µs
		P:Indir. (Data)	—	—	178 µs	12.2 µs	9.9 µs	9.9 µs
		P:Indir. (Bit)	—	—	270 µs	12.2 µs	9.9 µs	9.9 µs
	V: Bit Reg.	V:Data Reg.	184 µs	13.5 µs	130 µs	12.2 µs	4.8 µs	4.8 µs
		V:Bit Reg.	800 µs	13.5 µs	206 µs	12.2 µs	4.8 µs	4.8 µs
		K:Constant	193 µs	13.5 µs	139 µs	12.2 µs	3.4 µs	3.4 µs
		P:Indir. (Data)	—	—	252 µs	12.2 µs	9.9 µs	9.9 µs
		P:Indir. (Bit)	—	—	347 µs	12.2 µs	9.9 µs	9.9 µs
	P:Indir. (Data)	V:Data Reg.	—	—	174 µs	12.2 µs	9.9 µs	9.9 µs
		V:Bit Reg.	—	—	248 µs	12.2 µs	9.9 µs	9.9 µs
		K:Constant	—	—	182 µs	12.2 µs	8.3 µs	8.3 µs
		P:Indir. (Data)	—	—	296 µs	12.2 µs	14.3 µs	14.3 µs
		P:Indir. (Bit)	—	—	387 µs	12.2 µs	14.3 µs	14.3 µs
	P:Indir. (Bit)	V:Data Reg.	—	—	265 µs	12.2 µs	9.9 µs	9.9 µs
		V:Bit Reg.	—	—	341 µs	12.2 µs	9.9 µs	9.9 µs
		K:Constant	—	—	276 µs	12.2 µs	8.3 µs	8.3 µs
		P:Indir. (Data)	—	—	387 µs	12.2 µs	14.3 µs	14.3 µs
		P:Indir. (Bit)	—	—	480 µs	12.2 µs	14.3 µs	14.3 µs
STRN	1st	2nd						
	T, CT	V:Data Reg.	65 µs	13.5 µs	56 µs	12.2 µs	4.8 µs	4.8 µs
		V:Bit Reg.	180 µs	13.5 µs	130 µs	12.2 µs	4.8 µs	4.8 µs
		K:Constant	75 µs	13.5 µs	63 µs	12.2 µs	3.4 µs	3.4 µs
		P:Indir. (Data)	—	—	178 µs	12.2 µs	9.9 µs	9.9 µs
		P:Indir. (Bit)	—	—	270 µs	12.2 µs	9.9 µs	9.9 µs
	1st	2nd						
	V: Data Reg.	V:Data Reg.	65 µs	13.5 µs	56 µs	12.2 µs	4.8 µs	4.8 µs
		V:Bit Reg.	180 µs	13.5 µs	130 µs	12.2 µs	4.8 µs	4.8 µs
		K:Constant	77 µs	13.5 µs	63 µs	12.2 µs	3.4 µs	3.4 µs
		P:Indir. (Data)	—	—	178 µs	12.2 µs	9.9 µs	9.9 µs
		P:Indir. (Bit)	—	—	270 µs	12.2 µs	9.9 µs	9.9 µs
	V: Bit Reg.	V:Data Reg.	180 µs	13.5 µs	130 µs	12.2 µs	4.8 µs	4.8 µs
		V:Bit Reg.	298 µs	13.5 µs	206 µs	12.2 µs	4.8 µs	4.8 µs
		K:Constant	195 µs	13.5 µs	139 µs	12.2 µs	3.4 µs	3.4 µs
		P:Indir. (Data)	—	—	252 µs	12.2 µs	9.9 µs	9.9 µs
		P:Indir. (Bit)	—	—	347 µs	12.2 µs	9.9 µs	9.9 µs
	P:Indir. (Data)	V:Data Reg.	—	—	174 µs	12.2 µs	9.9 µs	9.9 µs
		V:Bit Reg.	—	—	248 µs	12.2 µs	9.9 µs	9.9 µs
		K:Constant	—	—	182 µs	12.2 µs	8.3 µs	8.3 µs
		P:Indir. (Data)	—	—	296 µs	12.2 µs	14.3 µs	14.3 µs
		P:Indir. (Bit)	—	—	387 µs	12.2 µs	14.3 µs	14.3 µs
	P:Indir. (Bit)	V:Data Reg.	—	—	265 µs	12.2 µs	9.9 µs	9.9 µs
		V:Bit Reg.	—	—	341 µs	12.2 µs	9.9 µs	9.9 µs
		K:Constant	—	—	276 µs	12.2 µs	8.3 µs	8.3 µs
		P:Indir. (Data)	—	—	387 µs	12.2 µs	14.3 µs	14.3 µs
		P:Indir. (Bit)	—	—	480 µs	12.2 µs	14.3 µs	14.3 µs

Comparative Boolean (cont.)			DL430		DL440		DL450	
Instruction	**Legal Data Types**		**Execute**	**Not Exe.**	**Execute**	**Not Exe.**	**Execute**	**Not Exe.**
OR	1st	2nd						
	T, CT	V:Data Reg.	64 µs	11.0 µs	46 µs	10.8 µs	4.8 µs	4.8 µs
		V:Bit Reg.	180 µs	11.0 µs	124 µs	10.8 µs	4.8 µs	4.8 µs
		K:Constant	74 µs	11.0 µs	57 µs	10.8 µs	3.4 µs	3.4 µs
		P:Indir. (Data)	—	—	168 µs	10.8 µs	9.9 µs	9.9 µs
		P:Indir. (Bit)	—	—	264 µs	10.8 µs	9.9 µs	9.9 µs
	1st	2nd						
	V: Data Reg.	V:Data Reg.	63 µs	13.5 µs	48 µs	10.8 µs	4.8 µs	4.8 µs
		V:Bit Reg.	180 µs	13.5 µs	122 µs	10.8 µs	4.8 µs	4.8 µs
		K:Constant	77 µs	13.5 µs	55 µs	10.8 µs	3.4 µs	3.4 µs
		P:Indir. (Data)	—	—	170 µs	10.8 µs	9.9 µs	9.9 µs
		P:Indir. (Bit)	—	—	262 µs	10.8 µs	9.9 µs	9.9 µs
	V: Bit Reg.	V:Data Reg.	180 µs	13.5 µs	122 µs	10.8 µs	4.8 µs	4.8 µs
		V:Bit Reg.	298 µs	13.5 µs	198 µs	10.8 µs	4.8 µs	4.8 µs
		K:Constant	195 µs	13.5 µs	131 µs	10.8 µs	3.4 µs	3.4 µs
		P:Indir. (Data)	—	—	244 µs	10.8 µs	9.9 µs	9.9 µs
		P:Indir. (Bit)	—	—	340 µs	10.8 µs	9.9 µs	9.9 µs
	P:Indir. (Data)	V:Data Reg.	—	—	165 µs	10.8 µs	9.9 µs	9.9 µs
		V:Bit Reg.	—	—	240 µs	10.8 µs	9.9 µs	9.9 µs
		K:Constant	—	—	175 µs	10.8 µs	8.3 µs	8.3 µs
		P:Indir. (Data)	—	—	288 µs	10.8 µs	14.3 µs	14.3 µs
		P:Indir. (Bit)	—	—	379 µs	10.8 µs	14.3 µs	14.3 µs
	P:Indir. (Bit)	V:Data Reg.	—	—	257 µs	10.8 µs	9.9 µs	9.9 µs
		V:Bit Reg.	—	—	333 µs	10.8 µs	9.9 µs	9.9 µs
		K:Constant	—	—	268 µs	10.8 µs	8.3 µs	8.3 µs
		P:Indir. (Data)	—	—	380 µs	10.8 µs	14.3 µs	14.3 µs
		P:Indir. (Bit)	—	—	473 µs	10.8 µs	14.3 µs	14.3 µs
ORN	1st	2nd						
	T, CT	V:Data Reg.	64 µs	11.0 µs	46 µs	10.8 µs	4.8 µs	4.8 µs
		V:Bit Reg.	178 µs	11.0 µs	124 µs	10.8 µs	4.8 µs	4.8 µs
		K:Constant	74 µs	11.0 µs	57 µs	10.8 µs	3.4 µs	3.4 µs
		P:Indir. (Data)	—	—	168 µs	10.8 µs	9.9 µs	9.9 µs
		P:Indir. (Bit)	—	—	264 µs	10.8 µs	9.9 µs	9.9 µs
	1st	2nd						
	V: Data Reg.	V:Data Reg.	63 µs	13.5 µs	48 µs	10.8 µs	4.8 µs	4.8 µs
		V:Bit Reg.	180 µs	13.5 µs	122 µs	10.8 µs	4.8 µs	4.8 µs
		K:Constant	77 µs	13.5 µs	55 µs	10.8 µs	3.4 µs	3.4 µs
		P:Indir. (Data)	—	—	170 µs	10.8 µs	9.9 µs	9.9 µs
		P:Indir. (Bit)	—	—	262 µs	10.8 µs	9.9 µs	9.9 µs
	V: Bit Reg.	V:Data Reg.	180 µs	13.5 µs	122 µs	10.8 µs	4.8 µs	4.8 µs
		V:Bit Reg.	298 µs	13.5 µs	198 µs	10.8 µs	4.8 µs	4.8 µs
		K:Constant	195 µs	13.5 µs	131 µs	10.8 µs	3.4 µs	3.4 µs
		P:Indir. (Data)	—	—	244 µs	10.8 µs	9.9 µs	9.9 µs
		P:Indir. (Bit)	—	—	340 µs	10.8 µs	9.9 µs	9.9 µs
	P:Indir. (Data)	V:Data Reg.	—	—	165 µs	10.8 µs	9.9 µs	9.9 µs
		V:Bit Reg.	—	—	240 µs	10.8 µs	9.9 µs	9.9 µs
		K:Constant	—	—	175 µs	10.8 µs	8.3 µs	8.3 µs
		P:Indir. (Data)	—	—	288 µs	10.8 µs	14.3 µs	14.3 µs
		P:Indir. (Bit)	—	—	379 µs	10.8 µs	14.3 µs	14.3 µs
	P:Indir. (Bit)	V:Data Reg.	—	—	257 µs	10.8 µs	9.9 µs	9.9 µs
		V:Bit Reg.	—	—	333 µs	10.8 µs	9.9 µs	9.9 µs
		K:Constant	—	—	268 µs	10.8 µs	8.3 µs	8.3 µs
		P:Indir. (Data)	—	—	380 µs	10.8 µs	14.3 µs	14.3 µs
		P:Indir. (Bit)	—	—	473 µs	10.8 µs	14.3 µs	14.3 µs

Comparative Boolean (cont.)			DL430		DL440		DL450	
Instruction	**Legal Data Types**		**Execute**	**Not Exe.**	**Execute**	**Not Exe.**	**Execute**	**Not Exe.**
AND	1st	2nd						
	T, CT	V:Data Reg.	62 µs	11.0 µs	46 µs	10.8 µs	4.8 µs	4.8 µs
		V:Bit Reg.	178 µs	11.0 µs	124 µs	10.8 µs	4.8 µs	4.8 µs
		K:Constant	73 µs	11.0 µs	57 µs	10.8 µs	3.4 µs	3.4 µs
		P:Indir. (Data)	—	—	168 µs	10.8 µs	9.9 µs	9.9 µs
		P:Indir. (Bit)	—	—	264 µs	10.8 µs	9.9 µs	9.9 µs
	1st	2nd						
	V: Data Reg.	V:Data Reg.	62 µs	11.0 µs	48 µs	10.8 µs	4.8 µs	4.8 µs
		V:Bit Reg.	178 µs	11.0 µs	122 µs	10.8 µs	4.8 µs	4.8 µs
		K:Constant	75 µs	11.0 µs	55 µs	10.8 µs	3.4 µs	3.4 µs
		P:Indir. (Data)	—	—	170 µs	10.8 µs	9.9 µs	9.9 µs
		P:Indir. (Bit)	—	—	262 µs	10.8 µs	9.9 µs	9.9 µs
	V: Bit Reg.	V:Data Reg.	178 µs	11.0 µs	122 µs	10.8 µs	4.8 µs	4.8 µs
		V:Bit Reg.	296 µs	11.0 µs	198 µs	10.8 µs	4.8 µs	4.8 µs
		K:Constant	192 µs	11.0 µs	131 µs	10.8 µs	3.4 µs	3.4 µs
		P:Indir. (Data)	—	—	244 µs	10.8 µs	9.9 µs	9.9 µs
		P:Indir. (Bit)	—	—	340 µs	10.8 µs	9.9 µs	9.9 µs
	P:Indir. (Data)	V:Data Reg.	—	—	165 µs	10.8 µs	9.9 µs	9.9 µs
		V:Bit Reg.	—	—	240 µs	10.8 µs	9.9 µs	9.9 µs
		K:Constant	—	—	175 µs	10.8 µs	8.3 µs	8.3 µs
		P:Indir. (Data)	—	—	288 µs	10.8 µs	14.3 µs	14.3 µs
		P:Indir. (Bit)	—	—	379 µs	10.8 µs	14.3 µs	14.3 µs
	P:Indir. (Bit)	V:Data Reg.	—	—	257 µs	10.8 µs	9.9 µs	9.9 µs
		V:Bit Reg.	—	—	333 µs	10.8 µs	9.9 µs	9.9 µs
		K:Constant	—	—	268 µs	10.8 µs	8.3 µs	8.3 µs
		P:Indir. (Data)	—	—	380 µs	10.8 µs	14.3 µs	14.3 µs
		P:Indir. (Bit)	—	—	473 µs	10.8 µs	14.3 µs	14.3 µs
ANDN	1st	2nd						
	T, CT	V:Data Reg.	62 µs	11.0 µs	46 µs	10.8 µs	4.8 µs	4.8 µs
		V:Bit Reg.	179 µs	11.0 µs	124 µs	10.8 µs	4.8 µs	4.8 µs
		K:Constant	73 µs	11.0 µs	57 µs	10.8 µs	3.4 µs	3.4 µs
		P:Indir. (Data)	—	—	168 µs	10.8 µs	9.9 µs	9.9 µs
		P:Indir. (Bit)	—	—	264 µs	10.8 µs	9.9 µs	9.9 µs
	1st	2nd						
	V: Data Reg.	V:Data Reg.	63 µs	13.5 µs	48 µs	10.8 µs	4.8 µs	4.8 µs
		V:Bit Reg.	180 µs	13.5 µs	122 µs	10.8 µs	4.8 µs	4.8 µs
		K:Constant	77 µs	13.5 µs	55 µs	10.8 µs	3.4 µs	3.4 µs
		P:Indir. (Data)	—	—	170 µs	10.8 µs	9.9 µs	9.9 µs
		P:Indir. (Bit)	—	—	262 µs	10.8 µs	9.9 µs	9.9 µs
	V: Bit Reg.	V:Data Reg.	180 µs	13.5 µs	122 µs	10.8 µs	4.8 µs	4.8 µs
		V:Bit Reg.	298 µs	13.5 µs	198 µs	10.8 µs	4.8 µs	4.8 µs
		K:Constant	195 µs	13.5 µs	131 µs	10.8 µs	3.4 µs	3.4 µs
		P:Indir. (Data)	—	—	244 µs	10.8 µs	9.9 µs	9.9 µs
		P:Indir. (Bit)	—	—	340 µs	10.8 µs	9.9 µs	9.9 µs
	P:Indir. (Data)	V:Data Reg.	—	—	165 µs	10.8 µs	9.9 µs	9.9 µs
		V:Bit Reg.	—	—	240 µs	10.8 µs	9.9 µs	9.9 µs
		K:Constant	—	—	175 µs	10.8 µs	8.3 µs	8.3 µs
		P:Indir. (Data)	—	—	288 µs	10.8 µs	14.3 µs	14.3 µs
		P:Indir. (Bit)	—	—	379 µs	10.8 µs	14.3 µs	14.3 µs
	P:Indir. (Bit)	V:Data Reg.	—	—	257 µs	10.8 µs	9.9 µs	9.9 µs
		V:Bit Reg.	—	—	333 µs	10.8 µs	9.9 µs	9.9 µs
		K:Constant	—	—	268 µs	10.8 µs	8.3 µs	8.3 µs
		P:Indir. (Data)	—	—	380 µs	10.8 µs	14.3 µs	14.3 µs
		P:Indir. (Bit)	—	—	473 µs	10.8 µs	14.3 µs	14.3 µs

Immediate Instructions

Immediate Instructions		DL430		DL440		DL450	
Instruction	Legal Data Types	Execute	Not Execute	Execute	Not Execute	Execute	Not Execute
STRI	X	22.0 µs	7.5 µs	15.6 µs	4.5 µs	128.0 µs	15.1 µs
STRNI	X	21.3 µs	7.5 µs	15.6 µs	4.5 µs	128.0 µs	15.3 µs
ORI	X	21.5 µs	5.2 µs	9.7 µs	4.8 µs	128.0 µs	14.8 µs
ORNI	X	20.8 µs	5.2 µs	9.7 µs	4.8 µs	128.0 µs	15.0 µs
ANDI	X	18.1 µs	5.2 µs	9.4 µs	2.1 µs	128.0 µs	14.8 µs
ANDNI	X	20.7 µs	5.2 µs	9.4 µs	2.1 µs	9.4 µs	2.1 µs
LDI	Y	—	—	—	—	406.3 µs	1.8 µs
OUTI	Y	27.3 µs	27.3 µs	18.0 µs	18.0 µs	135.0 µs	135.0 µs
OROUTI	Y	27.0 µs	27.0 µs	20.0 µs	20.0 µs	135.0 µs	23.5 µs
SETI	1st #: Y 2nd #: Y (N pt)	48.3 µs 24.6µs+ 23.7 xN	5.2 µs 5.2 µs	16.0 µs 18.0µs+ 15.9 xN	3.8 µs 3.8 µs	12.2 µs 139.7µs+ 0.6 xN	1.8 µs 2.2 µs
RSTI	1st #: Y 2nd #: Y (N pt)	47.1 µs 23.3µs+ 23.7 xN	5.2 µs 5.2 µs	15.1 µs 17.1µs+ 15.9 xN	3.8 µs 3.8 µs	12.2 µs 140.3µs+ 0.7 xN	1.8 µs 2.3 µs
LDIF	1st 2nd X K	—	—	252µs+ 16µs xN	3.8 µs	9.5 µs	2.3 µs
OUTIF	1st 2nd Y K	—	—	598µs+ 12µs xN	4.0 µs	12.5 µS	2.3 µs

Clock / Calendar Instructions

Clock / Calendar Instructions		DL430		DL440		DL450	
Instruction	Legal Data Types	Execute	Not Execute	Execute	Not Execute	Execute	Not Execute
DATE	V:Data Reg. V:Bit Reg.	—	—	135.0 µs 385.0 µs	4.0 µs 4.0 µs	21.3 µs 21.3 µs	1.9 µs 1.9 µs
TIME	V:Data Reg. V:Bit Reg.	—	—	121.0 µs 373.0 µs	4.0 µs 4.0 µs	13.2 µs 13.2 µs	1.9 µs 1.9 µs

Timer, Counter, and Shift Register Instructions

Timer, Counter, and Shift Register Instructions			DL430		DL440		DL450	
Instruction	**Legal Data Types**		**Execute**	**Not Execute**	**Execute**	**Not Execute**	**Execute**	**Not Execute**
TMR	1st	2nd						
	T	V:Data Reg.	63.9 µs	29.1 µs	45.0 µs	21.0 µs	40.0 µs	23.0 µs
		V:Bit Reg.	179.5 µs	29.1 µs	119.0 µs	21.0 µs	40.0 µs	23.0 µs
		K:Constant	76.3 µs	29.1 µs	52.4 µs	21.0 µs	35.7 µs	19.5 µs
		P:Indir. (Data)	—	—	200.7 µs	21.0 µs	51.8 µs	33.9 µs
		P:Indir. (Bit)	—	—	273.4 µs	21.0 µs	51.8 µs	33.9 µs
TMRF	1st	2nd						
	T	V:Data Reg.	63.9 µs	29.1 µs	45.0 µs	21.0 µs	77.8 µs	22.6 µs
		V:Bit Reg.	179.5 µs	29.1 µs	119.0 µs	21.0 µs	77.8 µs	22.6 µs
		K:Constant	76.3 µs	29.1 µs	52.4 µs	21.0 µs	69.8 µs	19.2 µs
		P:Indir. (Data)	—	—	200.7 µs	21.0 µs	83.4 µs	37.5 µs
		P:Indir. (Bit)	—	—	273.4 µs	21.0 µs	83.4 µs	37.5 µs
TMRA	1st	2nd						
	T	V:Data Reg.	74.0 µs	50.3 µs	50.6 µs	33.8 µs	66.0 µs	26.1 µs
		V:Bit Reg.	298.7 µs	275.0 µs	199.5 µs	182.7 µs	66.0 µs	26.1 µs
		K:Constant	85.0 µs	61.2 µs	58.3 µs	42.1 µs	61.8 µs	21.7 µs
		P:Indir. (Data)	—	—	228.0 µs	205.4 µs	76.8 µs	37.3 µs
		P:Indir. (Bit)	—	—	376.7 µs	354.0 µs	76.8 µs	37.3 µs
TMRAF	1st	2nd						
	T	V:Data Reg.	74.0 µs	50.3 µs	50.6 µs	33.8 µs	74.8 µs	26.1 µs
		V:Bit Reg.	298.7 µs	275.0 µs	199.5 µs	182.7 µs	74.8 µs	26.1 µs
		K:Constant	74.0 µs	74.0 µs	58.3 µs	42.1 µs	71.0 µs	21.7 µs
		P:Indir. (Data)	—	—	228.0 µs	205.4 µs	85.7 µs	37.3 µs
		P:Indir. (Bit)	—	—	376.7 µs	354.0 µs	85.7 µs	37.3 µs
CNT	1st	2nd						
	CT	V:Data Reg.	46.2 µs	38.2 µs	33.6 µs	29.8 µs	37.9 µs	24.6 µs
		V:Bit Reg.	161.4 µs	159.4 µs	107.6 µs	103.8 µs	37.9 µs	24.6 µs
		K:Constant	58.6 µs	50.6 µs	41.0 µs	37.2 µs	35.7 µs	21.6 µs
		P:Indir. (Data)	—	—	191.4 µs	186.7 µs	40.8 µs	35.7 µs
		P:Indir. (Bit)	—	—	264.7 µs	260.0 µs	40.8 µs	35.7 µs
SGCNT	1st	2nd						
	CT	V:Data Reg.	57.3 µs	44.2 µs	41.3 µs	32.9 µs	39.3 µs	23.8 µs
		V:Bit Reg.	172.5 µs	159.4 µs	119.5 µs	105.7 µs	39.3 µs	23.8 µs
		K:Constant	69.3 µs	56.2 µs	46.5 µs	40.4 µs	33.7 µs	20.3 µs
		P:Indir. (Data)	—	—	164.7 µs	156.7 µs	47.1 µs	34.7 µs
		P:Indir. (Bit)	—	—	263.4 µs	247.4 µs	47.1 µs	34.7 µs
UDC	1st	2nd						
	CT	V:Data Reg.	90.0 µs	60.6 µs	60.0 µs	41.9 µs	45.1 µs	34.8 µs
		V:Bit Reg.	314.7 µs	285.3 µs	209.0 µs	190.8 µs	45.1 µs	34.8 µs
		K:Constant	102.2 µs	72.8 µs	58.6 µs	50.5 µs	41.4 µs	30.9 µs
		P:Indir. (Data)	—	—	210.7 µs	198.7 µs	56.4 µs	45.9 µs
		P:Indir. (Bit)	—	—	358.7 µs	340.0 µs	56.4 µs	45.9 µs
SR	C (N points to shift)		36.8µs+ 2.3µsxN	17.9 µs	25.6µs+ 1.6µsxN	17.7 µs	8.9 µs+ 0.5 µsxN	7.7 µs

Accumulator / Data Stack Load and Output Instructions

Accumulator / Data Stack Load and Output Instructions		DL430		DL440		DL450	
Instruction	**Legal Data Types**	**Execute**	**Not Execute**	**Execute**	**Not Execute**	**Execute**	**Not Execute**
LD	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	102.0 µs 206.0 µs 112.0 µs 278.0 µs 391.0 µs	5.0 µs 5.0 µs 5.0 µs 5.0 µs 5.0 µs	97.0 µs 166.0 µs 110.0 µs 213.0 µs 272.0 µs	4.0 µs 4.0 µs 4.0 µs 4.0 µs 4.0 µs	6.4 µs 6.4 µs 12.7 µs 4.9 µs 4.9 µs	0.8 µs 0.8 µs 1.7 µs 0.8 µs 0.8 µs
LDD	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	106.0 µs 488.0 µs 112.0 µs 282.0 µs 670.0 µs	5.0 µs 5.0 µs 5.0 µs 5.0 µs 5.0 µs	101.0 µs 354.0 µs 112.0 µs 216.0 µs 460.0 µs	4.0 µs 4.0 µs 4.0 µs 4.0 µs 4.0 µs	7.2 µs 7.2 µs 13.5 µs 5.1 µs 5.1 µs	0.8 µs 0.8 µs 1.7 µs 0.8 µs 0.8 µs
LDF	1st 2nd X, Y, C, S K:Constant T, CT, SP, GX, GY	—	—	87µs+ 16µs x N	4.0 µs	10.5µs+ 3.45µs xN	2.3 µs
LDA	O: (Octal constant for address)	95.0 µs	5.0 µs	90.0 µs	4.0 µs	4.9 µs	0.8 µs
LDX	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	517.0 µs 816.0 µs — —	5.0 µs 5.0 µs — —	433.0 µs 583.0 µs — —	4.0 µs 4.0 µs — —	10.0 µs 10.0 µs 19.9 µs 19.9 µs	1.7 µs 1.7 µs 1.7 µs 1.7 µs
LDSX	K: Constant	—	—	90.0µs	4.0 µs	19.0 µs	2.3 µs
LDR	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	— — — — 	— — — — 	— — — — 	— — — — 	30.3 µs 30.3 µs 26.6 µs 39.9 µs 39.9 µs	1.8 µs 1.8 µs 1.8 µs 1.8 µs 1.8 µs
OUT	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	26.0 µs 181.0 µs 286.0 µs 538.0 µs	5.0 µs 5.0 µs 5.0 µs 5.0 µs	15.4 µs 96.7 µs 189.4 µs 334.6 µs	4.0 µs 4.0 µs 4.0 µs 4.0 µs	4.7 µs 4.7 µs 11.1 µs 11.1 µs	0.8 µs 0.8 µs 1.7 µs 1.7 µs
OUTD	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	35.0 µs 419.0 µs 296.0 µs 777.0 µs	5.0 µs 5.0 µs 5.0 µs 5.0 µs	21.4 µs 232.5 µs 196.0 µs 471.4 µs	4.0 µs 4.0 µs 4.0 µs 4.0 µs	5.4 µs 5.4 µs 11.7 µs 11.7 µs	0.8 µs 0.8 µs 1.8 µs 1.8 µs
OUTF	1st 2nd X, Y, C, S K:Constant T, CT, SP, GX, GY	—	—	52µs+ 12µs x N	4.0 µs	43.8 µs+ 6.2µs x N	2.3 µs
OUTX	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	551.0 µs 950.0 µs — —	5.0 µs 5.0 µs — —	356.0 µs 574.0 µs 471.0 µs 734.0 µs	4.0 µs 4.0 µs 4.0 µs 4.0 µs	14.1 µs 14.1 µs 23.8 µs 23.8 µs	1.8 µs 1.8 µs 1.8 µs 1.8 µs
POP	None	82.0 µs	5.0 µs	88.0 µs	4.0 µs	3.7 µs	4.0 µs

Accumulator Logic Instructions

Accumulator Logic Instructions		DL430		DL440		DL450	
Instruction	**Legal Data Types**	**Execute**	**Not Execute**	**Execute**	**Not Execute**	**Execute**	**Not Execute**
AND	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	101.0 µs 206.0 µs — —	5.0 µs 5.0 µs — —	66.0 µs 136.0 µs 183.4 µs 272.0 µs	4.0 µs 4.0 µs 4.0 µs 4.0 µs	4.9 µs 4.9 µs 11.1 µs 11.1 µs	0.8 µs 0.8 µs 1.7 µs 1.7 µs
ANDD	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	— — — — 115.0 µs	— — — — 5.0 µs	66.7 µs 323.4 µs 78.7 µs 186.0 µs 459.4 µs	4.0 µs 4.0 µs 4.0 µs 4.0 µs 4.0 µs	7.4 µs 7.4 µs 12.1 µs 3.6 µs 3.6 µs	1.7 µs 1.7 µs 1.7 µs 0.8 µs 0.8 µs
ANDF	1st 2nd X, Y, C, S K:Constant T, CT, SP, GX, GY	—	—	87µs+16µs x N	4.0 µs	3.9µs+ 3.4µs x N	2.3 µs
ANDS	None	—	—	77.4 µs	4.0 µs	5.0 µs	0.7 µs
OR	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	101.0 µs 206.0 µs — —	5.0 µs 5.0 µs — —	66.0 µs 136.0 µs 183.4 µs 272.0 µs	4.0 µs 4.0 µs 4.0 µs 4.0 µs	4.9 µs 4.9 µs 11.1 µs 11.1 µs	0.8 µs 0.8 µs 1.8 µs 1.8 µs
ORD	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	— — — — 115.0 µs	— — — — 5.0 µs	69.4 µs 328.4 µs 78.7 µs 186.0 µs 459.4 µs	4.0 µs 4.0 µs 4.0 µs 4.0 µs 4.0 µs	7.5 µs 7.5 µs 7.5 µs 3.7 µs 3.7 µs	1.8 µs 1.8 µs 1.8 µs 0.8 µs 0.8 µs
ORF	1st 2nd X, Y, C, S K:Constant T, CT, SP, GX, GY	—	—	87µs+16µs x N	4.0 µs	8.8µs+ 3.5µs x N	2.3 µs
ORS	None	—	—	77.4 µs	4.0 µs	5.0 µs	0.7 µs
XOR	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	101.0 µs 206.0 µs — —	5.0 µs 5.0 µs — —	33.0 µs 136.0 µs 183.4 µs 272.0 µs	4.0 µs 4.0 µs 4.0 µs 4.0 µs	5.0 µs 5.0 µs 11.2 µs 11.2 µs	0.8 µs 0.8 µs 1.8 µs 1.8 µs
XORD	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	— — — — 115.0 µs	— — — — 5.0 µs	69.4 µs 328.4 µs 78.7 µs 186.0 µs 459.4 µs	4.0 µs 4.0 µs 4.0 µs 4.0 µs 4.0 µs	7.5 µs 7.5 µs 12.1 µs 3.7 µs 3.7 µs	1.8 µs 1.8 µs 1.8 µs 0.8 µs 0.8 µs
XORF	1st 2nd X, Y, C, S K:Constant T, CT, SP, GX, GY	—	—	87µs+ 16µs x N	4.0 µs	8.8 µs+ 3.5µs x N	2.3 µs
XORS	None	—	—	77.3 µs	4.0 µs	5.0 µs	0.7 µs
CMP	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	56.0 µs 162.0 µs — —	5.0 µs 5.0 µs — —	36.0 µs 106.7 µs 158.7 µs 248.7 µs	4.0 µs 4.0 µs 4.0 µs 4.0 µs	6.1 µs 6.1 µs 12.4 µs 12.4 µs	0.8 µs 0.8 µs 1.8 µs 1.8 µs

Accumulator Logic Instructions (cont.)		DL430		DL440		DL450	
Instruction	**Legal Data Types**	**Execute**	**Not Execute**	**Execute**	**Not Execute**	**Execute**	**Not Execute**
CMPD	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	— — — — —	— — — — —	48.7 µs 312.7 µs 67.4 µs 181.4 µs 455.4 µs	4.0 µs 4.0 µs 4.0 µs 4.0 µs 4.0 µs	8.4 µs 8.4 µs 4.6 µs 13.0 µs 13.0 µs	1.8 µs 1.8 µs 0.8 µs 1.8 µs 1.8 µs
CMPF	1st 2nd X, Y, C, S K:Constant T, CT, SP, GX, GY	—	—	248µs+ 16µs x N	4.0 µs	12.4µs+ 3.5µs x N	2.3 µs
CMPR	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	— — — — —	— — — — —	— — — — —	— — — — —	39.6 µs 39.6 µs 29.7 µs 49.2 µs 49.2 µs	1.8 µs 1.8 µs 1.8 µs 1.8 µs 1.8 µs
CMPS	None	100.0 µs	5.0 µs	99.0 µs	4.0 µs	5.8 µs	0.7 µs

Bit Operation Instructions

Bit Operation Instructions		DL430		DL440		DL450	
Instruction	**Legal Data Types**	**Execute**	**Not Execute**	**Execute**	**Not Execute**	**Execute**	**Not Execute**
SUM	None	280.0 µs	5.0 µs	183.3 µs	4.0 µs	12.1 µs	1.6 µs
SHFL	V:Data Reg. (N bits) V:Bit Reg. (N bits) K:Constant (N bits)	52µs+ 21µs x N 157µs+ 21µs x N 63µs+ 21µs x N	5.0 µs 5.0 µs 5.0 µs	33µs+ 14µs x N 103µs+ 14µs x N 43µs+ 14µs x N	4.0 µs 4.0 µs 4.0 µs	9.8 µs+ .16µs x N 9.8 µs+ .16µs x N 7.9 µs+ .16µs x N	1.8 µs 1.8 µs 1.8 µs
SHFR	V:Data Reg. (N bits) V:Bit Reg. (N bits) K:Constant (N bits)	57µs+ 21µs x N 163µs+ 21µs x N 69µs+ 21µs x N	5.0 µs 5.0 µs 5.0 µs	36µs+ 14µs x N 107µs+ 14µs x N 43µs+ 14µs x N	4.0 µs 4.0 µs 4.0 µs	9.8 µs+ .16µs x N 9.8 µs+ .16µs x N 7.9 µs+ .16µs x N	1.8 µs 1.8 µs 1.8 µs
ROTL	V:Data Reg. (N bits) V:Bit Reg. (N bits) K:Constant (N bits)	66µs+ 25µs x N 171µs+ 25µs x N 78µs+ 25µs x N	5.0 µs 5.0 µs 5.0 µs	42µs+ 17µs x N 112µs+ 17µs x N 51µs+ 17s x N	4.0 µs 4.0 µs 4.0 µs	5.3 µs 5.3 µs 7.1 µs	1.9 µs 1.9 µs 1.9 µs
ROTR	V:Data Reg. (N bits) V:Bit Reg. (N bits) K:Constant (N bits)	69µs+ 25µs x N 174µs+ 25µs x N 81µs+ 25µs x N	5.0 µs 5.0 µs 5.0 µs	44µs+ 17µs x N 114µs+ 17µs x N 54µs+ 17s x N	4.0 µs 4.0 µs 4.0 µs	5.2 µs 5.2 µs 7.1 µs	1.9 µs 1.9 µs 1.9 µs
ENCO	None	107.0 µs	5.0 µs	69.4 µs	4.0 µs	23.5 µs	1.6 µs
DECO	None	61.0 µs	5.0 µs	39.4 µs	4.0 µs	6.5 µs	1.6 µs

Math Instructions

Math Instructions		DL430		DL440		DL450	
Instruction	**Legal Data Types**	**Execute**	**Not Execute**	**Execute**	**Not Execute**	**Execute**	**Not Execute**
ADD	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	308.0 µs 413.0 µs — —	5.0 µs 5.0 µs — —	203.4 µs 273.4 µs 318.0 µs 406.7 µs	4.0 µs 4.0 µs 4.0 µs 4.0 µs	43.8 µs 43.8 µs 50.2 µs 50.2 µs	0.8 µs 0.8 µs 1.8 µs 1.8 µs
ADDD	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	313.0 µs 694.0 µs 347.0 µs — —	5.0 µs 5.0 µs 5.0 µs — —	206.0 µs 460.7 µs 250.0 µs 374.0 µs 594.0 µs	4.0 µs 4.0 µs 4.0 µs 4.0 µs 4.0 µs	48.9 µs 48.9 µs 37.7 µs 53.6 µs 53.6 µs	1.8 µs 1.8 µs 0.8 µs 1.8 µs 1.8 µs
SUB	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	308.0 µs 413.0 µs — —	5.0 µs 5.0 µs — —	203.4 µs 273.4 µs 317.4 µs 405.4 µs	4.0 µs 4.0 µs 4.0 µs 4.0 µs	43.0 µs 43.0 µs 49.4 µs 49.4 µs	0.8 µs 0.8 µs 1.8 µs 1.8 µs
SUBD	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	313.0 µs 694.0 µs 347.0 µs — —	5.0 µs 5.0 µs 5.0 µs — —	206.7 µs 460.7 µs 250.7 µs 320.0 µs 592.7 µs	4.0 µs 4.0 µs 4.0 µs 4.0 µs 4.0 µs	48.2 µs 48.2 µs 36.7 µs 52.8 µs 52.8 µs	1.8 µs 1.8 µs 0.8 µs 1.8 µs 1.8 µs
MUL	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	458.0 µs 558.0 µs 469.0 µs — —	5.0 µs 5.0 µs 5.0 µs — —	300.0 µs 370.7 µs 342.7 µs 1020.7 µs 1108.7 µs	4.0 µs 4.0 µs 4.0 µs 4.0 µs 4.0 µs	159.0 µs 159.0 µs 153.0 µs 165.0 µs 165.0 µs	1.8 µs 1.8 µs 0.8 µs 1.8 µs 1.8 µs
MULD	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	— — — —	— — — —	— — — —	— — — —	480.1 µs 480.1 µs 484.0 µs 484.0 µs	1.9 µs 1.9 µs 1.9 µs 1.9 µs
DIV	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	6446.0 µs 6553.0 µs 6457.0 µs — —	5.0 µs 5.0 µs 5.0 µs — —	4358.0 µs 4446.7 µs 4361.4 µs 4490.7 µs 4578.0 µs	4.0 µs 4.0 µs 4.0 µs 4.0 µs 4.0 µs	217.0 µs 217.0 µs 211.0 µs 224.0 µs 224.0 µs	0.8 µs 0.8 µs 0.8 µs 1.8 µs 1.8 µs
DIVD	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	— — — —	— — — —	4428.0 µs 4682.0 µs 4543.0 µs 4806.0 µs	4.0 µs 4.0 µs 4.0 µs 4.0 µs	222.0 µs 222.0 µs 224.0 µs 224.0 µs	1.9 µs 1.9 µs 1.9 µs 1.9 µs
ADDB	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	143.0 µs 248.0 µs 145.0 µs — —	5.0 µs 5.0 µs 5.0 µs — —	94.0 µs 164.0 µs 100.0 µs 210.7 µs 298.7 µs	4.0 µs 4.0 µs 4.0 µs 4.0 µs 4.0 µs	11.6 µs 11.6.0 µs 17.8 µs 10.4 µs 10.4 µs	0.8 µs 0.8 µs 0.8 µs 1.8 µs 1.8 µs

Math Instructions (continued)		DL430		DL440		DL450	
Instruction	**Legal Data Types**	**Execute**	**Not Execute**	**Execute**	**Not Execute**	**Execute**	**Not Execute**
ADDBD	V:Data Reg.	—	—	90.0 µs	4.0 µs	14.2 µs	0.8 µs
	V:Bit Reg.	—	—	344.7 µs	4.0 µs	14.2 µs	0.8 µs
	K:Constant	—	—	99.4 µs	4.0 µs	10.4 µs	0.8 µs
	P:Indir. (Data)	—	—	206.7 µs	4.0 µs	18.8 µs	1.8 µs
	P:Indir. (Bit)	—	—	479.4 µs	4.0 µs	18.8 µs	1.8 µs
SUBB	V:Data Reg.	143.0 µs	5.0 µs	94.0 µs	4.0 µs	11.8 µs	0.8 µs
	V:Bit Reg.	248.0 µs	5.0 µs	164.0 µs	4.0 µs	11.8 µs	0.8 µs
	K:Constant	145.0 µs	5.0 µs	100.0 µs	4.0 µs	10.3 µs	0.8 µs
	P:Indir. (Data)	—	—	210.0 µs	4.0 µs	18.1 µs	1.8 µs
	P:Indir. (Bit)	—	—	298.0 µs	4.0 µs	18.1 µs	1.8 µs
SUBBD	V:Data Reg.	—	—	90.0 µs	4.0 µs	14.1 µs	0.8 µs
	V:Bit Reg.	—	—	344.7 µs	4.0 µs	14.1 µs	0.8 µs
	K:Constant	—	—	99.4 µs	4.0 µs	10.2 µs	0.8 µs
	P:Indir. (Data)	—	—	205.4 µs	4.0 µs	18.8 µs	1.8 µs
	P:Indir. (Bit)	—	—	478.7 µs	4.0 µs	18.8 µs	1.8 µs
MULB	V:Data Reg.	123.0 µs	5.0 µs	80.7 µs	4.0 µs	5.2 µs	0.8 µs
	V:Bit Reg.	228.0 µs	5.0 µs	150.7 µs	4.0 µs	5.2 µs	0.8 µs
	K:Constant	134.0 µs	5.0 µs	92.7 µs	4.0 µs	3.8 µs	0.8 µs
	P:Indir. (Data)	—	—	198.0 µs	4.0 µs	11.4 µs	1.8 µs
	P:Indir. (Bit)	—	—	286.0 µs	4.0 µs	11.4 µs	1.8 µs
DIVB	V:Data Reg.	4889.0 µs	5.0 µs	3261.4 µs	4.0 µs	22.8 µs	0.8 µs
	V:Bit Reg.	4995.0 µs	5.0 µs	3331.4 µs	4.0 µs	22.8 µs	0.8 µs
	K:Constant	4902.0 µs	5.0 µs	3273.4 µs	4.0 µs	21.3 µs	0.8 µs
	P:Indir. (Data)	—	—	3380.0 µs	4.0 µs	29.1 µs	1.8 µs
	P:Indir. (Bit)	—	—	3468.0 µs	4.0 µs	29.1 µs	1.8 µs
ADDR	V:Data Reg.	—	—	—	—	46.8 µs	1.8 µs
	V:Bit Reg.	—	—	—	—	46.8 µs	1.8 µs
	K:Constant	—	—	—	—	33.8 µs	1.8 µs
	P:Indir. (Data)	—	—	—	—	56.5 µs	1.8 µs
	P:Indir. (Bit)	—	—	—	—	56.5 µs	1.8 µs
SUBR	V:Data Reg.	—	—	—	—	46.8 µs	1.8 µs
	V:Bit Reg.	—	—	—	—	46.8 µs	1.8 µs
	K:Constant	—	—	—	—	33.8 µs	1.8 µs
	P:Indir. (Data)	—	—	—	—	56.5 µs	1.8 µs
	P:Indir. (Bit)	—	—	—	—	56.5 µs	1.8 µs
MULR	V:Data Reg.	—	—	—	—	44.4 µs	1.8 µs
	V:Bit Reg.	—	—	—	—	44.4 µs	1.8 µs
	K:Constant	—	—	—	—	33.8 µs	1.8 µs
	P:Indir. (Data)	—	—	—	—	54.1 µs	1.8 µs
	P:Indir. (Bit)	—	—	—	—	54.1 µs	1.8 µs
DIVR	V:Data Reg.	—	—	—	—	49.0 µs	1.8 µs
	V:Bit Reg.	—	—	—	—	49.0 µs	1.8 µs
	K:Constant	—	—	—	—	38.4 µs	1.8 µs
	P:Indir. (Data)	—	—	—	—	58.3 µs	1.8 µs
	P:Indir. (Bit)	—	—	—	—	58.3 µs	1.8 µs

Math Instructions (continued)		DL430		DL440		DL450	
Instruction	**Legal Data Types**	**Execute**	**Not Execute**	**Execute**	**Not Execute**	**Execute**	**Not Execute**
ADDBS	None	—	—	97.4 µs	4.0 µs	11.4 µs	0.7 µs
SUBBS	None	—	—	96.7 µs	4.0 µs	11.7 µs	0.7 µs
MULBS	None	—	—	92.7 µs	4.0 µs	5.1 µs	0.7 µs
DIVBS	None	—	—	3072.0 µs	4.0 µs	12.2 µs	0.7 µs
ADDF	1st 2nd X, Y, C, S K:Constant T, CT, SP, GX, GY	—	—	224µs+ 16µs x N	4.0 µs	50.1 µs+ 3.5 µs x N	2.3 µs
SUBF	1st 2nd X, Y, C, S K:Constant T, CT, SP, GX, GY	—	—	224µs+ 16µs x N	4.0 µs	49.2 µs+ 3.5 µs x N	2.3 µs
MULF	1st 2nd X, Y, C, S K:Constant T, CT, SP, GX, GY	—	—	325µs+ 8µs x N	4.0 µs	163.1 µs+ 3.4 µs x N	2.3 µs
DIVF	1st 2nd X, Y, C, S K:Constant T, CT, SP, GX, GY	—	—	4472µs+ 8µs x N	4.0 µs	20.9 µs+ 3.4 µs x N	2.3 µs
ADDS	None	321.0 µs	5.0 µs	265.0 µs	4.0 µs	46.5 µs	0.6 µs
SUBS	None	324.0 µs	5.0 µs	265.0 µs	4.0 µs	45.6 µs	0.7 µs
MULS	None	475.0 µs	5.0 µs	392.0 µs	4.0 µs	362.5 µs	0.7 µs
DIVS	None	6463.0 µs	5.0 µs	4061.0 µs	4.0 µs	501.8 µs	0.7 µs
INC	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	119.0 µs 381.0 µs — —	5.0 µs 5.0 µs — —	78.0 µs 230.0 µs 196.0 µs 372.0 µs	4.0 µs 4.0 µs 4.0 µs 4.0 µs	22.6 µs 22.6 µs 29.0 µs 29.0 µs	0.8 µs 0.8 µs 1.9 µs 1.9 µs
DEC	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	119.0 µs 381.0 µs — —	5.0 µs 5.0 µs — —	78.0 µs 230.0 µs 210.7 µs 298.7 µs	4.0 µs 4.0 µs 4.0 µs 4.0 µs	22.3 µs 22.3 µs 28.6 µs 28.6 µs	0.8 µs 0.8 µs 1.9 µs 1.9 µs
INCB	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	41.0 µs 303.0 µs — —	5.0 µs 5.0 µs — —	26.0 µs 178.0 µs 143.4 µs 329.0 µs	4.0 µs 4.0 µs 4.0 µs 4.0 µs	7.3 µs 7.3 µs 13.5 µs 13.5 µs	0.8 µs 0.8 µs 1.9 µs 1.9 µs
DECB	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	41.0 µs 303.0 µs — —	5.0 µs 5.0 µs — —	26.0 µs 178.0 µs 142.0 µs 330.7 µs	4.0 µs 4.0 µs 4.0 µs 4.0 µs	7.3 µs 7.3 µs 13.5 µs 13.5 µs	0.8 µs 0.8 µs 1.9 µs 1.9 µs

Math Instructions (continued)		DL430		DL440		DL450	
Instruction	Legal Data Types	Execute	Not Execute	Execute	Not Execute	Execute	Not Execute
SQRT	None	—	—	—	—	197.6 µs	1.6 µs
SQRTR	None	—	—	—	—	61.96 µs	1.6 µs
SIN	None	—	—	—	—	274.7 µs	1.6 µs
SINR	None	—	—	—	—	110.96 µs	1.6 µs
COS	None	—	—	—	—	280.4 µs	1.6 µs
COSR	None	—	—	—	—	116.0 µs	1.6 µs
TAN	None	—	—	—	—	294.1 µs	1.6 µs
TANR	None	—	—	—	—	145.2 µs	1.6 µs
ASIN	None	—	—	—	—	349.6 µs	1.6 µs
ASINR	None	—	—	—	—	230.5 µs	1.6 µs
ACOS	None	—	—	—	—	355.5 µs	1.6 µs
ACOSR	None	—	—	—	—	237.8 µs	1.6 µs
ATAN	None	—	—	—	—	274.9 µs	1.6 µs
ATANR	None	—	—	—	—	155.5 µs	1.6 µs

Number Conversion Instructions

Number Conversion Instructions		DL430		DL440		DL450	
Instruction	Legal Data Types	Execute	Not Execute	Execute	Not Execute	Execute	Not Execute
BIN	None	409.0 µs	5.0 µs	107.4 µs	4.0 µs	127.3 µs	1.6 µs
BCD	None	409.0 µs	5.0 µs	152.0 µs	4.0 µs	125.3 µs	1.6 µs
INV	None	46.0 µs	5.0 µs	15.0 µs	4.0 µs	2.9 µs	1.6 µs
BCDCPL	None	—	—	232.7µs	4.0 µs	35.3µs	1.6 µs
ATH	V:Data Reg. (1 word) V:Bit Reg. (1 word)	— —	— —	1494.7µs 1910.0µs	4.0 µs 4.0 µs	14.3 µs 14.3 µs	1.9 µs 1.9 µs
HTA	V:Data Reg. (1 word) V:Bit Reg. (1 word)	— —	— —	1489.4µs 1960.7µs	4.0 µs 4.0 µs	14.3 µs 14.3 µs	1.9 µs 1.9 µs
SEG	None	101.0 µs	5.0 µs	64.0 µs	4.0 µs	6.9 µs	1.6 µs
GRAY	None	—	—	176.0 µs	4.0 µs	69.1 µs	1.6 µs
SFLDGT	None	—	—	224.0 µs	4.0 µs	21.6 µs	1.6 µs
RAD	None	—	—	—	—	175.0 µs	1.6 µs
RADR	None	—	—	—	—	42.5 µs	1.6 µs
DEG	None	—	—	—	—	176.2 µs	1.6 µs
DEGR	None	—	—	—	—	42.4 µs	1.6 µs
BTOR	None	—	—	—	—	11.1 µs	1.6 µs
RTOB	None	—	—	—	—	34.2 µs	1.6 µs

Table Instructions

Table Instructions		DL430		DL440		DL450	
Instruction	**Legal Data Types**	**Execute**	**Not Execute**	**Execute**	**Not Execute**	**Execute**	**Not Execute**
FILL	V:Data Reg. V:Bit Reg. K:Constant	— — — —	— — — —	596µs+ 74µs x N 904µs+ 74µs x N 608µs+ 74µs x N	4.0µs 4.0µs 4.0µs	13.6 µs+ 4.4µs x N 13.6µs+ 1.4µs x N 17.3µs+ 4.2µs x N	1.9 µs 1.9 µs 1.9 µs
FIND	V:Data Reg. V:Bit Reg. K:Constant	— — — —	— — — —	372µs+ 85µs x N 442µs+ 85µs x N 384µs+ 85µs x N	4.0µs 4.0µs 4.0µs	23.0µs+ 3.1µs x N 23.0µs+ 3.1µs x N 20.2µs+ 3.1µs x N	1.9 µs 1.9 µs 1.9 µs
FDGT	V:Data Reg. V:Bit Reg. K:Constant	— — —	— — —	1028.6µs 1098.7µs 1066.7µs	4.0µs 4.0µs 4.0µs	25.9 µs 25.9 µs 26.2 µs	1.9 µs 1.9 µs 1.9 µs
MOV	V:Data Reg. V:Bit Reg.	— —	— —	1767.0µs 3188.0µs	4.0µs 4.0µs	24.1 µs 24.1 µs	1.9 µs 1.9 µs
TTD	V	—	—	748.7µs	4.0µs	29.8 µs	1.9 µs
RFB	V	—	—	747.4µs	4.0µs	21.0 µs	1.9 µs
STT	V K	— —	— —	722.7 µs 784.0 µs	4.0µs 4.0µs	27.7 µs 24.9 µs	1.9 µs 1.9 µs
RFT	V	—	—	1548.0µs	4.0µs	22.1 µs	1.9 µs
ATT	V K	— —	— —	2725.4µs 2734.4µs	4.0µs 4.0µs	25.0 µs 22.1 µs	1.9 µs 1.9 µs
MOVMC	Move V:Data Reg. to MC Move V:Bit Reg. to MC Move from MC to V:Data Reg. Move from MC to V:Bit Reg.	— — — —	— — — —	1332.7µs 2215.4µs 818.0µs 1394.0µs	4.0µs 4.0µs 4.0µs 4.0µs	6.0 µs 6.0 µs 22.7 µs 22.7 µs	1.9 µs 1.9 µs 1.9 µs 1.9 µs
LDLBL	K	—	—	62.0 µs	4.0 µs	7.6 µs	1.9 µs

CPU Control Instructions

CPU Control Instructions		DL430		DL440		DL450	
Instruction	**Legal Data Types**	**Execute**	**Not Exe.**	**Execute**	**Not Exe.**	**Execute**	**Not Exe.**
NOP	None	0	0	0	0	1 µs	1 µs
END	None	15.5 µs	15.5 µs	11.6 µs	11.6 µs	8.5 µs	8.5 µs
STOP	None	26.0 µs	5.0 µs	17.4 µs	4.0 µs	6.7 µs	1.6 µs
BREAK	None	—	—	717.0 µs	4.0 µs	15.3 µs	1.6 µs
RSTWT	None	22.0 µs	5.0 µs	14.7 µs	4.0 µs	4.0 µs	1.6 µs

Program Control Instructions

Program Control Instructions		DL430		DL440		DL450	
Instruction	Legal Data Types	Execute	Not Exe.	Execute	Not Exe.	Execute	Not Exe.
GOTO	K	—	—	18.7 µs	4.0 µs	5.1 µs	4.6 µs
LBL	K	—	—	0 µs	0 µs	0 µs	0 µs
FOR	V, K	—	—	32.7 µs	4.0 µs	59.6 µs	7.1 µs
NEXT	None	—	—	57.4 µs	4.0 µs	80.0 µs	0 µs
GTS	K	—	—	38.7 µs	4.0 µs	20.3 µs	5.2 µs
SBR	K	—	—	0 µs	0 µs	0.8 µs	0 µs
RTC	None	—	—	37.4 µs	4.0 µs	6.1 µs	6.1 µs
RT	None	—	—	35.4 µs	4.0 µs	5.1 µs	0 µs
MLS	K (1–7)	16.3 µs	16.3 µs	16.6 µs	16.6 µs	2.1 µs	2.1 µs
MLR	K (0–7)	20.0 µs	20.0 µs	13.4 µs	13.4 µs	2.0 µs	2.0 µs

Interrupt Instructions

Interrupt Instructions		DL430		DL440		DL450	
Instruction	Legal Data Types	Execute	Not Exe.	Execute	Not Exe.	Execute	Not Exe.
ENI	None	12.0 µs	5.0 µs	8.0 µs	4.0 µs	9.0 µs	1.6 µs
DISI	None	12.0 µs	5.0 µs	8.0 µs	4.0 µs	11.7 µs	1.6 µs
INT	0 (0–17)	0 µs	0 µs	0 µs	0 µs	0 µs	0 µs
IRTC	None	180.0 µs	5.0 µs	121.4 µs	4.0 µs	0.7 µs	0.7 µs
IRT	None	180.0 µs	—	120.0 µs	—	1.4 µs	—

RLL*PLUS* Instructions

RLL*PLUS* Instructions		DL430		DL440		DL450	
Instruction	Legal Data Types	Execute	Not Exe.	Execute	Not Exe.	Execute	Not Exe.
ISG	S	44.0 µs	42.0 µs	22.0 µs	20.0 µs	22.2 µs	21.0 µs
SG	S	44.0 µs	42.0 µs	22.0 µs	20.0 µs	22.2 µs	21.2 µs
JMP	S	14.0 µs	5.0 µs	10.7 µs	4.0 µs	20.7 µs	4.1 µs
NJMP	S	15.0 µs	5.0 µs	12.7 µs	4.0 µs	21.3 µs	4.5 µs
CV	S	—	—	30.0 µs	7.0 µs	13.8 µs	13.8 µs
CVJMP	S (N stages)	—	—	20 µs + 6 µs x N	7.0 µs	12.3 µs	12.3 µs
BCALL	C	—	—	12.0 µs	10.0 µs	19.4 µs	19.4 µs
BLK	C	—	—	21.0 µs	14.0 µs	18.3 µs	15.6 µs
BEND	None	—	—	6.0 µs	0 µs	7.8 µs	0 µs

Intelligent I/O Instructions

Intelligent Module Instructions		DL430		DL440		DL450	
Instruction	**Legal Data Types**	**Execute**	**Not Exe.**	**Execute**	**Not Exe.**	**Execute**	**Not Exe.**
RD	V:Data Reg. V:Bit Reg.	1130+ 123xN µs 1150+ 172xN µs	5.0 µs 5.0 µs	754+ 82xN µs 766+ 105xN µs	4.0 µs 4.0 µs	109.6 µs 109.6 µs	1.9 µs 1.9 µs
WT	V:Data Reg. V:Bit Reg.	1840+ 150xN µs 1875+ 180xN µs	5.0 µs 5.0 µs	896+ 110xN µs 917+ 120xN µs	4.0 µs 4.0 µs	109.8 µs 109.8 µs	1.9 µs 1.9 µs

Network Instructions

Network Instructions		DL430		DL440		DL450	
Instruction	**Legal Data Types**	**Execute**	**Not Exe.**	**Execute**	**Not Exe.**	**Execute**	**Not Exe.**
RX	X, Y, C, T, CT, GX,, GY SP, S V:Data Reg. V:Bit Reg.	760.0 µs 760.0 µs 780.0 µs	5.0 µs 5.0 µs 5.0 µs	488.0 µs 488.0 µs 488.0 µs	4.0 µs 4.0 µs 4.0 µs	111.8 µs 111.8 µs 111.8 µs	2.3 µs 2.3 µs 2.3 µs
WX	X, Y, C, T, CT, GX,, GY SP, S V:Data Reg. V:Bit Reg.	Source 755+ 12xN µs	5.0 µs 5.0 µs 5.0 µs	Source 503+ 8xN µs	4.0 µs 4.0 µs 4.0 µs	111.8 µs 111.8 µs 111.8 µs	2.3 µs 2.3 µs 2.3 µs
PRINT	ASCII	—	—	—	—	104.0 µs	2.2 µs

Message Instructions

Message Instructions		DL430		DL440		DL450	
Instruction	**Legal Data Types**	**Execute**	**Not Exe.**	**Execute**	**Not Exe.**	**Execute**	**Not Exe.**
FAULT	V:Data Reg. V:Bit Reg. K:Constant	164.0 µs 266.0 µs 158.0 µs	5.0 µs 5.0 µs 5.0 µs	107.0 µs 178.0 µs 158.7 µs	4.0 µs 4.0 µs 4.0 µs	107.3 µs 107.3 µs 98.1 µs	2.3 µs 2.3 µs 2.3 µs
DLBL	K	—	—	0 µs	0 µs	0 µs	0 µs
NCON	K	—	—	0 µs	0 µs	0 µs	0 µs
ACON	K	—	—	0 µs	0 µs	0 µs	0 µs

Drum Instructions

Drum Instructions		DL430		DL440		DL450	
Instruction	**Legal Data Types**	**Execute**	**Not Exe.**	**Execute**	**Not Exe.**	**Execute**	**Not Exe.**
DRUM	CT	—	—	—	—	340.0 µs	62.6 µs
EDRUM	CT	—	—	—	—	243.0 µs	100.0 µs
MDRMD	CT	—	—	—	—	206.0 µs	142.00 µs
MDRMW	CT	—	—	—	—	150.0 µs	94.00 µs